ECE 523/421 - Analog Electronics:
University of New Mexico

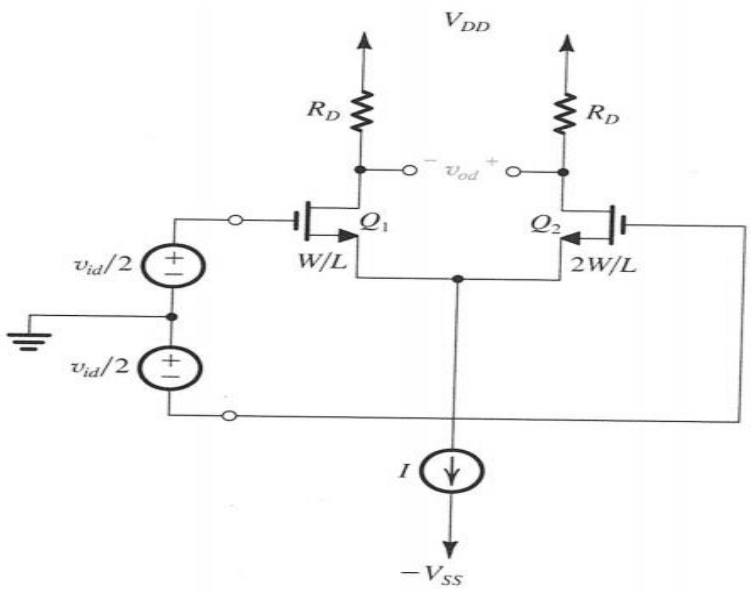
Problem 9.24

A design error has resulted in a gross mismatch in the circuit of Fig. P9.24. Specifically, Q2 has twice the W/L ratio of Q1. If vid is a small sine-wave signal, find:

(a) ID1 and ID2.

(b) VOV for each of Q1 and Q2.

(c) The differential gain Ad in terms of RD, I, and VOV.



a) For Id

$$I_{D1} = \frac{1}{2}k_n{}'\left(\frac{W}{L}\right)(V_{GS1} - V_t)^2$$

$$I_{D2} = \frac{1}{2}k_n{}'\left(2\frac{W}{L}\right)(V_{GS2} - V_t)^2$$

From the circuit

$$V_{GS1} - V_t = V_{GS2} - V_t$$

$$I_{D2} = \frac{1}{2}k_n{}'\left(2\frac{W}{L}\right)(V_{GS2} - V_t)^2$$

$$(V_{GS2} - V_t)^2 = \frac{I_{D2}}{\frac{1}{2}k_n{}'\left(2\frac{W}{L}\right)}$$

Substituting that on equation for Id1

$$I_{D1} = \frac{1}{2} k_n{}' \left(\frac{W}{L}\right) \frac{I_{D2}}{\frac{1}{2} k_n{}' \left(2\frac{W}{L}\right)}$$

$$I_{D1} = \frac{I_{D2}}{2}$$

Also

$$I = I_{D1} + I_{D2}$$

Solving for this equations

$$I_{D1} = \frac{I}{3}$$

$$I_{D2} = \frac{2I}{3}$$

b) Substituting values

$$I_{D1} = \frac{1}{2} k_n{}' \left(\frac{W}{L}\right) (V_{OV1})^2$$

$$\frac{I}{3} = \frac{1}{2} k_n{}' \left(\frac{W}{L}\right) (V_{OV1})^2$$

$$V_{OV1} = \sqrt{\frac{2}{3} \frac{I}{k_n{}' \left(\frac{W}{L}\right)}}$$

$$I_{D2} = \frac{1}{2} k_n{}' \left(2\frac{W}{L}\right) (V_{OV2})^2$$

$$\frac{2I}{3} = \frac{1}{2} k_n{}' \left(2\frac{W}{L}\right) (V_{OV2})^2$$

$$V_{OV2} = \sqrt{\frac{2}{3} \frac{I}{k_n{}' \left(\frac{W}{L}\right)}}$$

Problem 9.61

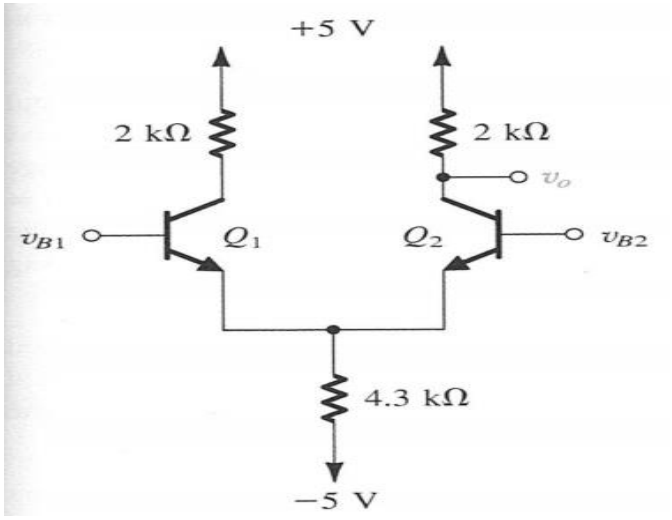
The differential amplifier circuit of Fig. P9.61 utilizes a resistor connected to the negative power supply to establish the bias current I.

(a) For *vB*1= *vid*/2 and *vB*2=−*vid* /2, where *vid* is a small signal with zero average, find the magnitude of the differential gain, |*vo*/*vid*|.

(b) For *vB*1=*vB*2=*vicm*, where *vicm* has a zero average, find the magnitude of the common-mode gain, |*vo*/*vicm*|.

(c) Calculate the CMRR.

(d) If *vB*1=0.1 sin 2*π* ×60*t* + 0.005 sin 2*π* ×1000*t*, volts, and *vB*2=0.1 sin 2*π* ×60*t*−0.005 sin 2*π* ×1000*t*, volts, find *vo*.



a) For calculating the current of the resistor

$$I = \frac{5 - 0.7}{4.3\ k\Omega}$$

$$I = 1\ mA$$

$$I_E = \frac{I}{2}$$

$$I_E = 0.5\ mA$$

$$r_e = \frac{V_T}{I_E}$$

$$r_e = 50\ \Omega$$

$$A_d = \frac{\alpha}{2r_e}(R_C)$$

$$A_d = \frac{\alpha}{2r_e}(R_C)$$

$$A_d = 20\ V/V$$

b) For the gain in common mode

$$A_{cm} = \frac{\alpha}{2R_e + r_e}(R_C)$$

$$A_{cm} = \frac{1}{2(4.3k) + 50}(2\ k)$$

$$A_{cm} = 0.23\ V/V$$

c) For the common-mode reject ratio

$$CMRR = 20\ \log\left(\frac{A_d}{A_{cm}}\right)$$

$$CMRR = 20\ \log\left(\frac{29}{0.23}\right)$$

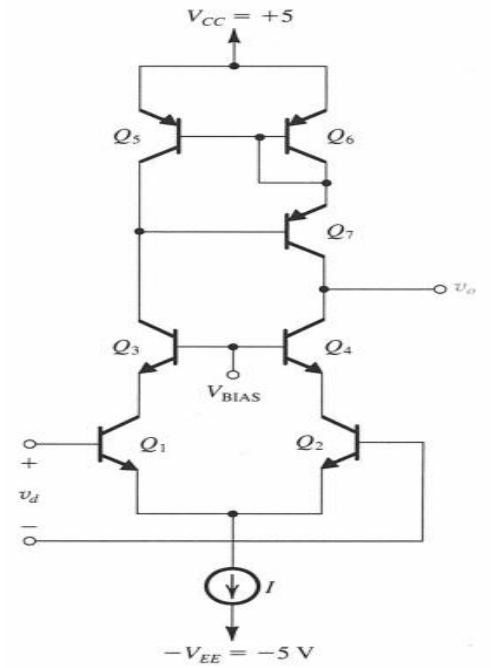
$$CMRR = 38.8\ dB$$

Problem 9.98

Figure P9.98 shows a differential cascode amplifier with an active load formed by a Wilson current mirror. Utilizing the expressions derived in Chapter 8 for the output resistance of a bipolar cascode and the output resistance of the Wilson mirror, and assuming all transistors to be identical, show that the differential voltage gain Ad is given approximately by

$$\boldsymbol{A_d = \frac{1}{3}(\beta g_m r_o)}$$

Evaluate Ad for the case of β = 100 and VA =20 V.



$$A_{vo} = G_m(R_o)$$

$$G_m = g_m$$

$$R_o = R_{oc}||R_{ow}$$

$$R_{oc} = Output\ resistance\ of\ cascode\ stage = \beta r_o$$

$$R_{ow} = Output\ resistance\ of\ wilson\ stage = \frac{\beta r_o}{2}$$

$$R_o = \beta r_o || \frac{\beta r_o}{2}$$

$$R_o = \frac{\beta r_o}{3}$$

$$A_{vo} = g_m\left(\frac{\beta r_o}{3}\right)$$

$$A_{vo} = \frac{1}{3}(\beta g_m r_o)$$

Evaluating

$$g_m = \frac{I/2}{V_t}$$

$$r_o = \frac{V_A}{I/2}$$

$$A_{vo} = \frac{\beta}{3}\frac{I/2}{V_t}\frac{V_A}{I/2}$$

$$A_{vo} = \frac{\beta}{3}\frac{V_A}{V_t}$$

$$A_{vo} = 26666.7$$

$$A_{vo} = 88.5\ dB$$

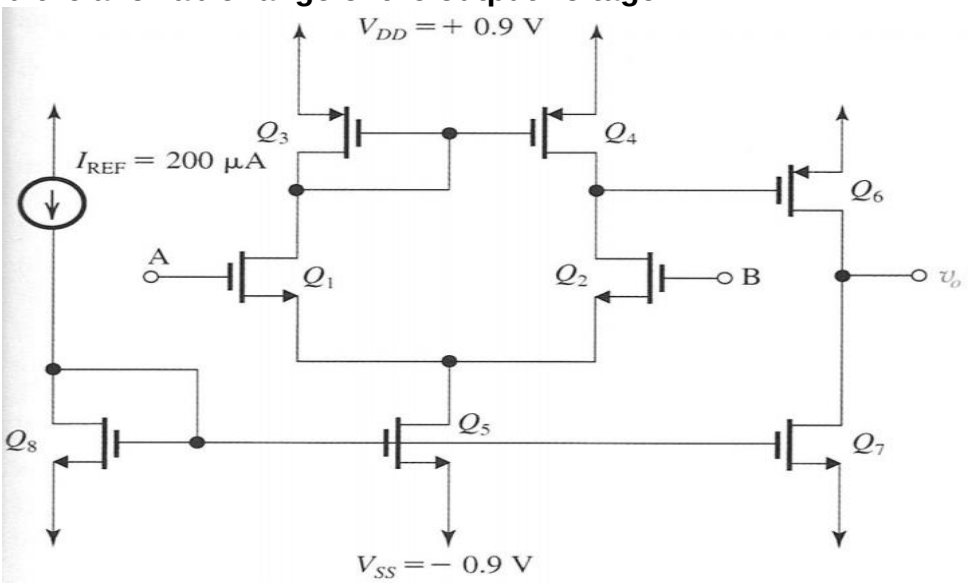
Problem 9.114

The two-stage CMOS op amp in Fig. P9.114 is fabricated in a 0.18-μm technology having k'n= 4k'p = 400 μA/V2, Vtn =−Vtp = 0.4 V.

(a) With A and B grounded, perform a dc design that will result in each of Q1, Q2, Q3, and Q4 conducting a drain current of 100 μA and each of Q6 and Q7 a current of 200 μA. Design so that all transistors operate at 0.2-V overdrive voltages. Specify the W/L ratio required for each MOSFET. Present your results in tabular form. What is the dc voltage at the output (ideally)?

(b) Find the input common-mode range.

(c) Find the allowable range of the output voltage.



a) For obtaining the W/L ratios we will use the current equation

$$I_{D1,2} = \frac{1}{2} k_n' \left(\frac{W}{L}\right)_{1,2} (V_{OV})^2$$

$$100\ \mu = \frac{1}{2} 400\mu \left(\frac{W}{L}\right)_{1,2} (0.2)^2$$

$$\left(\frac{W}{L}\right)_{1,2} = 12.5$$

$$I_{D3,4} = \frac{1}{2} k_p' \left(\frac{W}{L}\right)_{3,4} (V_{OV})^2$$

$$100\ \mu = \frac{1}{2} 100\mu \left(\frac{W}{L}\right)_{3,4} (0.2)^2$$

$$\left(\frac{W}{L}\right)_{3,4} = 50$$

$$I_{D6} = \frac{1}{2} k_p{}' \left(\frac{W}{L}\right)_6 (V_{OV})^2$$
$$200\ \mu = \frac{1}{2} 100\mu \left(\frac{W}{L}\right)_6 (0.2)^2$$
$$\left(\frac{W}{L}\right)_6 = 100$$

$$I_{D5,7,8} = \frac{1}{2} k_n{}' \left(\frac{W}{L}\right)_{5,7,8} (V_{OV})^2$$
$$200\ \mu = \frac{1}{2} 400\mu \left(\frac{W}{L}\right)_{5,7,8} (0.2)^2$$
$$\left(\frac{W}{L}\right)_{5,7,8} = 25$$

IF A and B are connected to ground, the output voltage should be 0V

b) For the input common-mode range
Lower limit

$$V_{LOW} = -0.9 + 0.4 + 0.4$$
$$V_{LOW} = -0.1V$$

Upper limit

$$V_{HIGH} = 0.9 - 0.2$$
$$V_{HIGH} = 0.7V$$

C) For the allowable range of the output voltage
Lower limit

$$V_{LOW} = -V_{SS} + V_{OV}$$
$$V_{LOW} = -0.7V$$

Upper limit

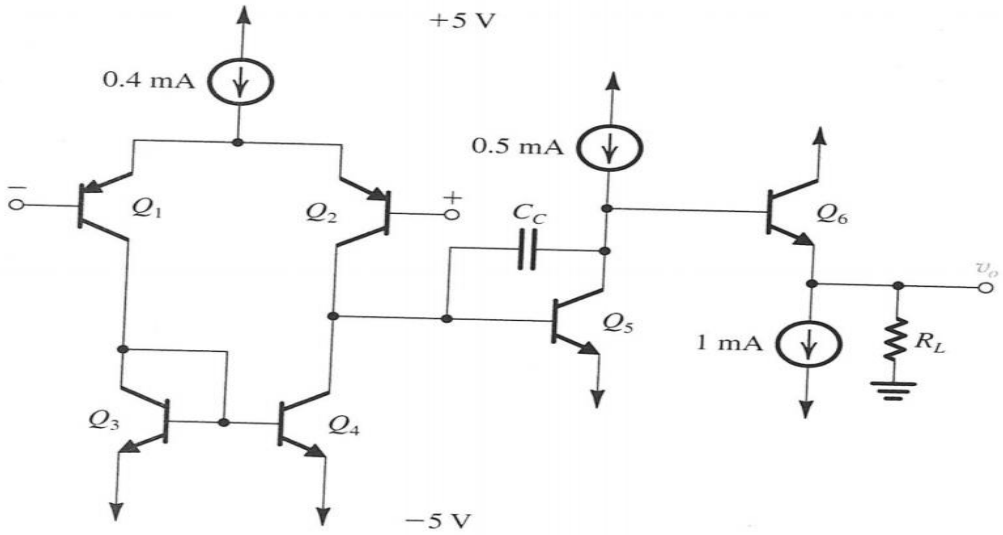
$$V_{HIGH} = V_{DD} - V_{OV}$$
$$V_{HIGH} = 0.7V$$

Problem 119

Figure P9.119 shows a bipolar op-amp circuit that resembles the CMOS op amp of Fig. 9.40. Here, the input differential pair Q1–Q2 is loaded in a current mirror formed by Q3 and Q4. The second stage is formed by the current-source-loaded common-emitter transistor Q5. Unlike the CMOS circuit, here there is an output stage formed by the emitter follower Q6. The function of capacitor CC will be explained later, in Chapter 11. All transistors have β = 100, |VBE| = 0.7 V, and ro =∞.

(a) For inputs grounded and output held at 0 V (by negative feedback, not shown) find the emitter currents of all transistors.

(b) Calculate the gain of the amplifier with RL =1 kΩ.



a) Finding the emitter currents

$$I_{E1} = I_{E2} = 0.2\ mA$$
$$I_{E3} = I_{E4} \approx 0.2\ mA$$
$$I_{E5} \approx 0.5\ mA$$

Since the output is held at 0V

$$I_{E6} = 1\ mA$$

b) Calculating the gain

$$r_e = \frac{V_T}{I_E}$$
$$r_{e1} = r_{e2} = \frac{25\ mV}{0.2\ mA} = 125\Omega$$
$$r_{e5} = \frac{25\ mV}{0.5\ mA} = 50\Omega$$
$$r_{e6} = \frac{25\ mV}{1\ mA} = 25\Omega$$

The gain for the first stage

$$G_{m1} = g_{m1} = \frac{1}{r_{e1}} = 8\,{}^{mA}/_{V}$$

$$A_{1st} = G_{m1}(\beta + 1)r_{e5}$$

$$A_{1st} = 40.4\,V/V$$

For the second stage

The common-emitter

$$A_5 = g_{m5}R_{e5} \cong \frac{-\beta R_L}{r_{e5}}$$

$$A_5 = \frac{-100\ x\ 1k}{50}$$

$$A_5 = -2000\,V/V$$

For the emitter follower

$$A_6 \approx 1$$

$$A_{2nd} = A_5\ x\ A_6$$

$$A_{2nd} = -2000\,V/V$$

$$A_{total} = A_{1st}\ x\ A_{2nd}$$

$$A_{total} = -80800$$

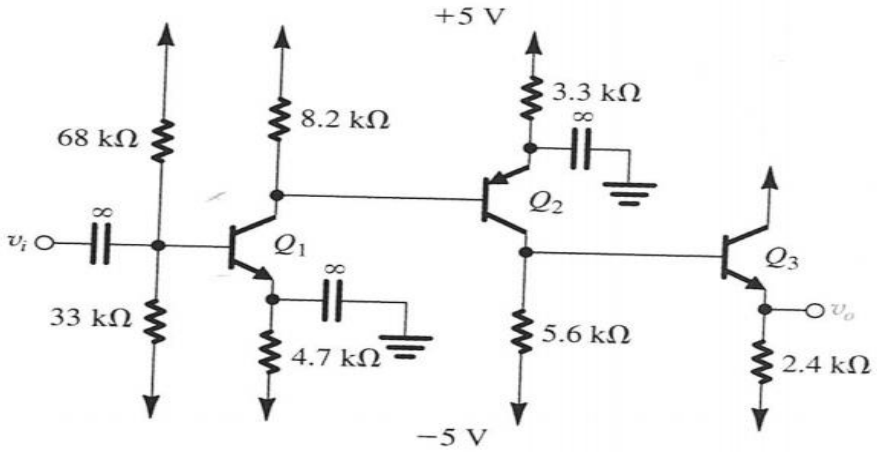
Problem 9.124

Figure P9.124 shows a three-stage amplifier in which the stages are directly coupled. The amplifier, however, utilizes bypass capacitors, and, as such, its frequency response falls off at low frequencies. For our purposes here, we shall assume that the capacitors are large enough to act as perfect short circuits at all signal frequencies of interest.

(a) Find the dc bias current in each of the three transistors. Also find the dc voltage at the output. Assume |*VBE*| = 0.7V, *β* = 100, and neglect the Early effect.

(b) Find the input resistance and the output resistance.

(c) Use the current-gain method to evaluate the voltage gain *vo*/*vi*.



a) Calculating the voltage of the node and Applying KVL

$$V_x = \frac{10V\ x\ 33k}{33k + 68k} = 3.3V$$

$$33k||68k = 22.2k$$

$$I_{E1} = \frac{3.3 - 0.7}{4.7k + \frac{22.2k}{101}}$$

$$I_{E1} = 0.53\ mA$$

$$I_{C1} = 0.52\ mA$$

$$V_{C1} = 5 - 0.52mA\ x\ 8.2k = 0.74V$$

$$I_{E2} = \frac{5 - 0.7 - 0.74}{3.3k}$$

$$I_{E2} = 1.07\ mA$$

$$I_{C2} = 1.06\ mA$$

$$V_{C2} = 1.06mA\ x\ 5.6k - 5 = 0.94V$$

$$v_o = 0.94 - 0.7 = 0.24$$

$$I_{E3} = \frac{0.24 - (-5)}{2.4k}$$
$$I_{E3} = 2.2mA$$
$$I_{C3} = 2.1mA$$

b) The input and output resistance

$$R_{in} = 68k||33k||r_{\Pi 1}$$
$$r_{\Pi 1} = \frac{\beta}{g_{m1}} = \frac{100}{20.8\,m} = 4.8\ k\Omega$$
$$R_{in} = 3.95\ k\Omega$$

$$R_{out} = 2.4k||\left(r_{e3} + \frac{5.6k}{\beta + 1}\right)$$
$$R_{out} = 2.4k||\left(11.4 + \frac{5.6k}{101}\right)$$
$$R_{out} = 65.3\ \Omega$$

c) The voltage gain

$$\frac{I_{C1}}{v_i} = g_{m1} = 20.8\,{}^{mA}/_{V}$$
$$\frac{I_{b2}}{I_{C1}} = \frac{8.2k}{8.2k + r_{\Pi 2}} = \frac{8.2k}{8.2k + 2.4k} = 0.77$$
$$\frac{I_{C2}}{I_{b2}} = \beta = 100$$
$$\frac{I_{b3}}{I_{C2}} = \frac{5.6k}{5.6k + (\beta + 1)(r_{e3} + 2.4k)} = 0.02248$$
$$\frac{I_{e3}}{I_{b3}} = \beta + 1 = 101$$
$$v_o = I_{e3}\ x\ 2.4k$$
$$\frac{v_o}{v_i} = 2.4k\ x\ 101\ x\ 0.02248\ x\ 100\ x\ 0.77\ x\ 20.8$$
$$\frac{v_o}{v_i} = 8730\ V/V$$