(e) Sketch a Bode plot for the gain of this amplifier. What does the plot tell you about the gain at dc? Does this make sense? Why or why not?

D 10.6 Figure P10.6 shows a CS amplifier biased by a constant-current source I. Let $R_{sig} = 0.5\ \text{M}\Omega$, $R_G = 2\ \text{M}\Omega$, $g_m = 3\ \text{mA/V}$, $R_D = 20\ \text{k}\Omega$, and $R_L = 10\ \text{k}\Omega$. Find A_M. Also, design the coupling and bypass capacitors to locate the three low-frequency poles at 100 Hz, 10 Hz, and 1 Hz. Use a minimum total capacitance, with the capacitors specified only to a single significant digit. What value of f_L results?

D 10.7 Figure P10.7 shows a current-biased CE amplifier operating at 100 μA from ±3-V power supplies. It employs

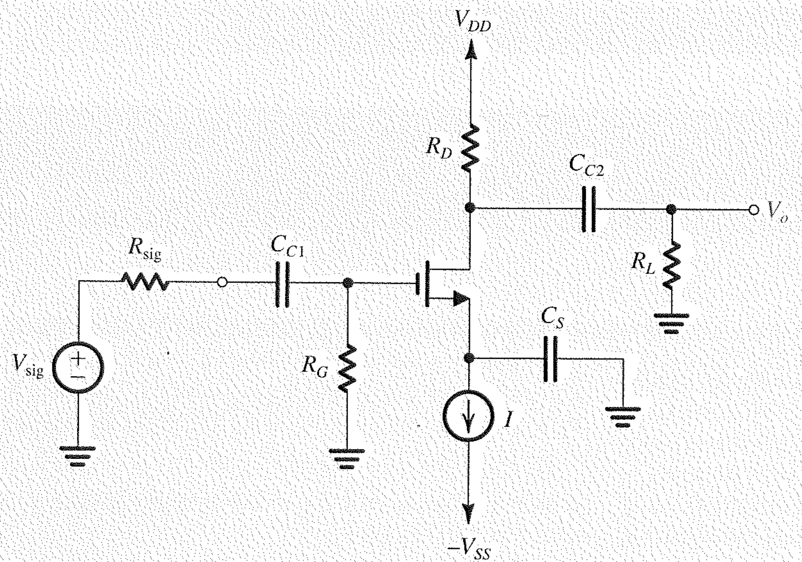

Figure P10.6

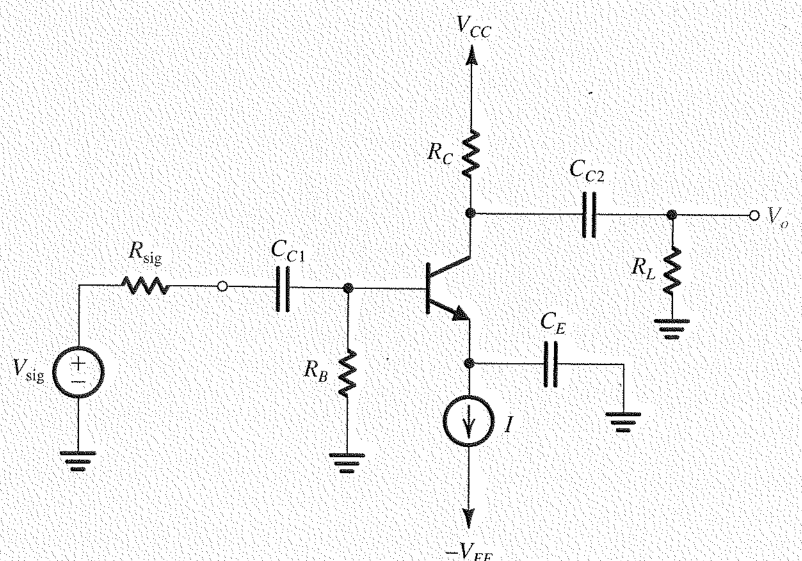

Figure P10.7

Section 10.4: Useful Tools for the Analysis of the High-Frequency Response of Amplifiers

10.51 A direct-coupled amplifier has a low-frequency gain of 40 dB, poles at 2 MHz and 20 MHz, a zero on the negative real axis at 200 MHz, and another zero at infinite frequency. Express the amplifier gain function in the form of Eqs. (10.70) and (10.71), and sketch a Bode plot for the gain magnitude. What do you estimate the 3-dB frequency f_H to be?

10.52 An amplifier with a dc gain of 60 dB has a single-pole, high-frequency response with a 3-dB frequency of 100 kHz.

(a) Give an expression for the gain function $A(s)$.
(b) Sketch Bode diagrams for the gain magnitude and phase.
(c) What is the gain–bandwidth product?
(d) What is the unity-gain frequency?
(e) If a change in the amplifier circuit causes its transfer function to acquire another pole at 1 MHz, sketch the resulting gain magnitude and specify the unity-gain frequency. Note that this is an example of an amplifier with a unity-gain bandwidth that is different from its gain–bandwidth product.

10.53 Consider an amplifier whose $F_H(s)$ is given by

$$F_H(s) = \frac{1}{\left(1+\frac{s}{\omega_{P1}}\right)\left(1+\frac{s}{\omega_{P2}}\right)}$$

with $\omega_{P1} < \omega_{P2}$. Find the ratio ω_{P2}/ω_{P1} for which the value of the 3-dB frequency ω_H calculated using the dominant-pole approximation differs from that calculated using the root-sum-of-squares formula (Eq. 10.77) by:

(a) 10%
(b) 1%

10.54 The high-frequency response of a direct-coupled amplifier having a dc gain of -1000 V/V incorporates zeros at ∞ and 10^4 rad/s (one at each frequency) and poles at 10^3 rad/s and 10^5 rad/s (one at each frequency). Write an expression for the amplifier transfer function. Find ω_H using

(a) the dominant-pole approximation
(b) the root-sum-of-squares approximation (Eq. 10.77).

If a way is found to lower the frequency of the finite zero to 10^3 rad/s, what does the transfer function become? What is the 3-dB frequency of the resulting amplifier?

10.55 A direct-coupled amplifier has a dominant pole at 1000 rad/s and three coincident poles at a much higher frequency. These nondominant poles cause the phase lag of the amplifier at high frequencies to exceed the 90° angle due to the dominant pole. It is required to limit the excess phase at $\omega = 10^7$ rad/s to 30° (i.e., to limit the total phase angle to $-120°$). Find the corresponding frequency of the nondominant poles.

10.56 An IC CS amplifier has $g_m = 2$ mA/V, $C_{gs} = 30$ fF, $C_{gd} = 5$ fF, $C_L = 30$ fF, $R'_{sig} = 10$ kΩ, and $R'_L = 20$ kΩ. Use the method of open-circuit time constants to obtain an estimate for f_H. Also, find the frequency of the transmission zero, f_Z.

10.57 For a particular amplifier modeled by the circuit of Fig. 10.18(a), $g_m = 5$ mA/V, $R_{sig} = 150$ kΩ, $R_G = 0.65$ MΩ, $R'_L = 10$ kΩ, $C_{gs} = 2$ pF, and $C_{gd} = 0.5$ pF. There is also a load capacitance of 30 pF. Find the corresponding midband voltage gain, the open-circuit time constants, and an estimate of the 3-dB frequency.

10.58 Consider the high-frequency response of an amplifier consisting of two identical stages in cascade, each with an input resistance of 10 kΩ and an output resistance of 2 kΩ. The two-stage amplifier is driven from a 10-kΩ source and drives a 1-kΩ load. Associated with each stage is a parasitic input capacitance (to ground) of 10 pF and a parasitic output capacitance (to ground) of 2 pF. Parasitic capacitances of 10 pF and 7 pF also are associated with the signal-source and load connections, respectively. For this arrangement, find the three poles and estimate the 3-dB frequency f_H.

10.59 A CS amplifier that can be represented by the equivalent circuit of Fig. 10.24 has $C_{gs} = 2$ pF, $C_{gd} = 0.1$ pF, $C_L = 2$ pF, $g_m = 4$ mA/V, and $R'_{sig} = R'_L = 20$ kΩ. Find the midband gain A_M, the input capacitance C_{in} using the Miller approximation, and hence an estimate of the 3-dB frequency f_H. Also, obtain another estimate of f_H using open-circuit time constants. Which of the two estimates is more appropriate and why?

D 10.60 For a CS amplifier with $g_m = 5$ mA/V, $C_{gs} = 5$ pF, $C_{gd} = 1$ pF, $C_L = 5$ pF, $R'_{sig} = 10$ kΩ, and $R'_L = 10$ kΩ, find τ_H and f_H. What is the percentage of τ_H that is caused by the interaction of R'_{sig} with the input capacitance? To what value must R'_{sig} be lowered in order to double f_H?

D 10.61 For the CS amplifier in Example 10.8, find the value of the additional capacitance to be connected at the output node in order to lower f_H to 100 MHz.

SIM = Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem

10.91 A differential amplifier is biased by a current source having an output resistance of 1 MΩ and an output capacitance of 1 pF. The differential gain exhibits a dominant pole at 2 MHz. What are the poles of the CMRR?

10.92 A current-mirror-loaded MOS differential amplifier is biased with a current source $I = 0.2$ mA. The two NMOS transistors of the differential pair are operating at $V_{OV} = 0.2$ V, and the PMOS devices of the mirror are operating at $|V_{OV}| = 0.2$ V. The Early voltage $V_{An} = |V_{Ap}| = 10$ V. The total capacitance at the input node of the mirror is 0.1 pF and that at the output node of the amplifier is 0.2 pF. Find the dc value and the frequencies of the poles and zero of the differential voltage gain.

10.93 Consider the current-mirror-loaded CMOS differential amplifier of Fig. 10.37(a) for the case of all transistors operated at the same $|V_{OV}|$ and having the same $|V_A|$. Also let the total capacitance at the output node (C_L) be four times the total capacitance at the input node of the current mirror C_m. Give expressions for A_d, f_{P1}, f_{P2}, and f_Z. Hence show that $f_{P2}/f_{P1} = 4A_d$ and $f_t = g_m/2\pi C_L$. For $V_A = 20$ V, $V_{OV} = 0.2$ V, $I = 0.2$ mA, $C_L = 100$ fF, and $C_m = 25$ fF, find the dc value of A_d, and the value of f_{P1}, f_t, f_{P2}, and f_Z and sketch a Bode plot for $|A_d|$.

***10.94** For the current mirror in Fig. P10.94, derive an expression for the current transfer function $I_o(s)/I_i(s)$ taking into account the BJT internal capacitances and neglecting r_x and r_o. Assume the BJTs to be identical. Observe that a signal ground appears at the collector of Q_2. If the mirror is biased at 1 mA and the BJTs at this operating point are characterized by $f_T = 500$ MHz, $C_\mu = 2$ pF, and $\beta_0 = 100$, find the frequencies of the pole and zero of the transfer function.

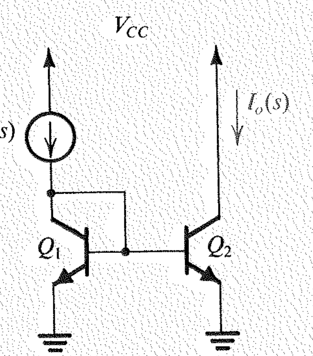

Figure P10.94

Section 10.8: Other Wideband Amplifier Configurations

10.95 Consider the case of a discrete-circuit CS amplifier in which a source-degeneration resistance is utilized to control the bandwidth. Assume that r_o is very large and C_L is negligibly small. Adapt the formulas given in the text for this case and thus give the expressions for A_M and f_H. Let $R_{sig} = 100$ kΩ, $g_m = 5$ mA/V, $R_L = 5$ kΩ, $C_{gs} = 10$ pF, and $C_{gd} = 2$ pF. Find $|A_M|$, f_H, and the gain–bandwidth product for these three cases: $R_s = 0$, 100 Ω, and 200 Ω.

10.96 A CS amplifier is specified to have $g_m = 5$ mA/V, $r_o = 40$ kΩ, $C_{gs} = 2$ pF, $g_{gd} = 0.1$ pF, $C_L = 1$ pF, $R_{sig} = 20$ kΩ, and $R_L = 40$ kΩ.

(a) Find the low-frequency gain A_M, and use open-circuit time constants to estimate the 3-dB frequency f_H. Hence determine the gain–bandwidth product.

(b) If a 400-Ω resistance is connected in the source lead, find the new values of $|A_M|$, f_H, and the gain–bandwidth product.

D 10.97 (a) Use the approximate expression in Eq. (10.156) to determine the gain–bandwidth product of a CS amplifier with a source-degeneration resistance. Assume $C_{gd} = 0.2$ pF and $R_{sig} = 100$ kΩ.

(b) If a low-frequency gain of 20 V/V is required, what f_H corresponds?

(c) For $g_m = 5$ mA/V, $A_0 = 100$ V/V, and $R_L = 20$ kΩ, find the required value of R_s.

10.98 For the CS amplifier with a source-degeneration resistance R_s, show for $R_{sig} \gg R_s$, $r_o \gg R_s$, and $R_L = r_o$ that

$$A_M = \frac{-A_0}{2+k}$$

and

$$\tau_H \simeq \frac{C_{gs}R_{sig}}{1+(k/2)} + C_{gd}R_{sig}\left(1+\frac{A_0}{2+k}\right) + (C_L + C_{gd})r_o\left(\frac{1+k}{2+k}\right)$$

where $k \equiv g_m R_s$

D *10.99 It is required to generate a table of $|A_M|$, f_H, and f_t versus $k \equiv g_m R_s$ for a CS amplifier with a source-degeneration resistance R_s. The table should have entries for $k = 0, 1, 2, \ldots, 15$. The amplifier is specified to have $g_m = 5$ mA/V, $r_o = 40$ kΩ, $R_L = 40$ kΩ, $R_{sig} = 20$ kΩ, $C_{gs} = 2$ pF, $C_{gd} = 0.1$ pF, and $C_L = 1$ pF. Use the formulas

***10.106** Figure P10.106 shows an amplifier formed by cascading two CS stages. Note that the input bias voltage is not shown. Each of Q_1 and Q_2 is operated at an overdrive voltage of 0.2 V, and $|V_A| = 10$ V. The transistor capacitances are as follows: $C_{gs} = 20$ fF, $C_{gd} = 5$ fF, and $C_{db} = 5$ fF. The signal-source resistance $R_{sig} = 10$ kΩ.

(a) Find the dc voltage gain.
(b) Use the method of open-circuit time constants to determine an estimate for the 3-dB frequency f_H.

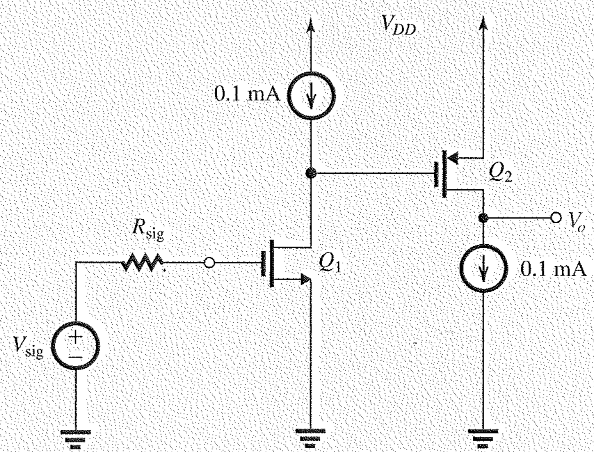

Figure P10.106

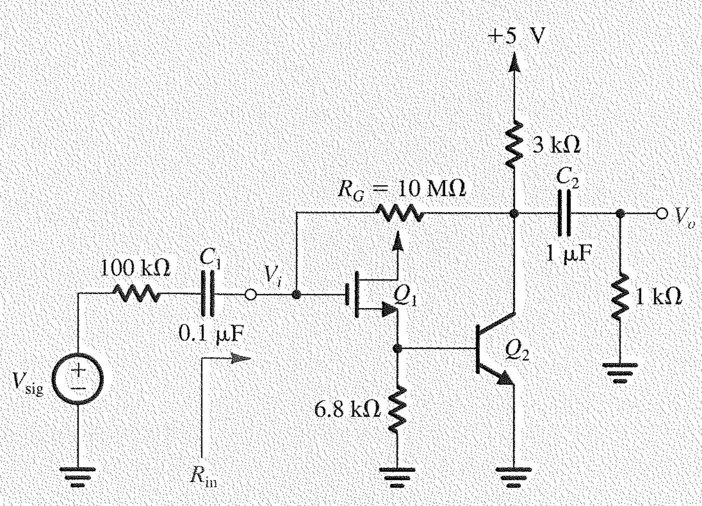

Figure P10.107

****10.107** Consider the BiCMOS amplifier shown in Fig. P10.107. The BJT has $|V_{BE}| = 0.7$ V, $\beta = 200$, $C_\mu = 0.8$ pF, and $f_T = 600$ MHz. The NMOS transistor has $V_t = 1$ V, $k_n' W/L = 2$ mA/V^2, and $C_{gs} = C_{gd} = 1$ pF.

(a) Consider the dc bias circuit. Neglect the base current of Q_2 in determining the current in Q_1. Find the dc bias currents in Q_1 and Q_2, and show that they are approximately 100 μA and 1 mA, respectively.
(b) Evaluate the small-signal parameters of Q_1 and Q_2 at their bias points.
(c) Consider the circuit at midband frequencies. First, determine the small-signal voltage gain V_o/V_i. (Note that R_G can be neglected in this process.) Then use Miller's theorem on R_G to determine the amplifier input resistance R_{in}. Finally, determine the overall voltage gain V_o/V_{sig}. Assume r_o of both transistors to be very large.
(d) Consider the circuit at low frequencies. Determine the frequency of the poles due to C_1 and C_2, and hence estimate the lower 3-dB frequency, f_L.
(e) Consider the circuit at higher frequencies. Use Miller's theorem to replace R_G with a resistance at the input. (The one at the output will be too large to matter.) Use open-circuit time constants to estimate f_H.

*****10.108** In each of the six circuits in Fig. P10.108, let $\beta = 100$, $C_\mu = 2$ pF, and $f_T = 400$ MHz, and neglect r_x and r_o. Calculate the midband gain A_M and the 3-dB frequency f_H.