ECE 523/421 – Analog Electronics

Lecture 1: Introduction to Analog Electronics

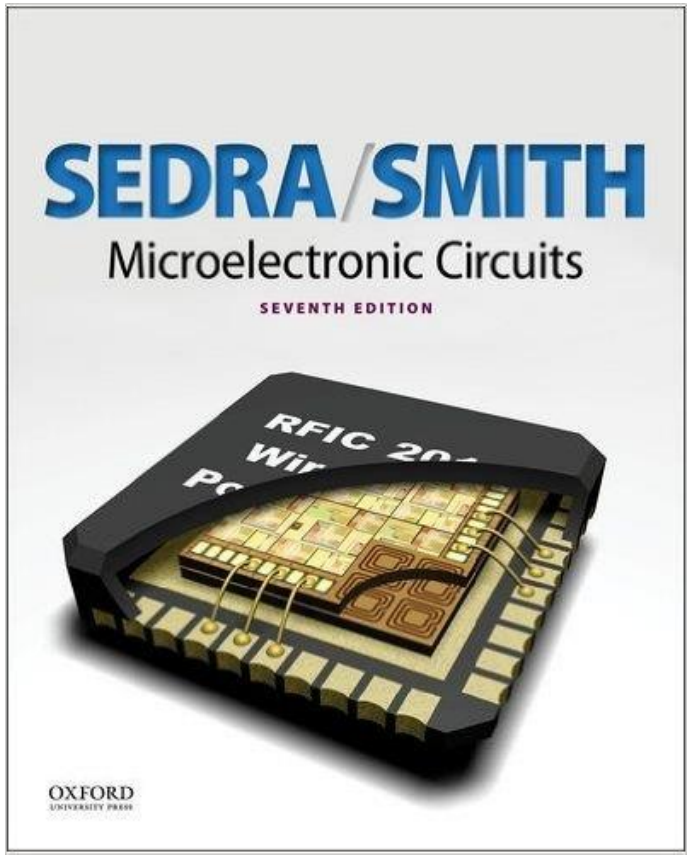
Payman Zarkesh-Ha

Office: ECE Bldg. 230B
Office hours: Tuesday 2:00-3:00PM or by appointment
E-mail: pzarkesh@unm.edu

Textbook and Background

- Main reference material is your notes in the class and the handouts
- The main textbook is:
  - A. Sedra and K. Smith, "Microelectronic Circuits", 7th edition, Oxford University Press, 2014, ISBN-978-0199339136
- Lecture Notes: combination of slides, homework and announcements
  - Slides will be posted on the class webpage
  - Class webpage: *www.unm.edu/~pzarkesh/ECE523*

Textbooks and Outline



- Basic CMOS Amplifiers
- Basic BJT Amplifiers
- Cascode Amplifiers
- Current Mirrors
- Differential Amplifiers
- Frequency Response
- Feedback Analysis
- Stability Analysis with Feedback
- Frequency Compensation
- Power Amplifiers

Grading Policy

- **Your grade in the course will be comprised of:**

  ECE523 and ECE421 Students

  - **Homework (20%)**
  - **Design Project (20%)**
  - **Tests (30%)**
  - **Final Exam (30%)**

- **There will be 2 midterm tests, but only 1 will be considered and the worst test will be ignored. Therefore, there is no makeup tests or exams.**

- **Final letter grade will be based on curve and class performance**

- **Your participation in class is very important**

- **Suggestions for success:**

  - **Participate in the class and ask questions**
  - **Read the textbook**
  - **Work on problems**

Homework Policy

- Homework will be assigned for each week. Please refer to the class website for the homework assignments.
- Homework due at the beginning of the lecture. No exception!
- Solutions will be posted on the class website as soon as it is available.
- Late homework and projects will not be accepted

Course Project

- There will be design project assigned including:
  - Circuit Design at the transistor level
  - SPICE simulation to confirm functionality and measure specs
  - No layout is needed for this project
- The design problem will be an individual project.
- Project grade will be based on:
  - Quality of report
  - Meeting all the required specifications
  - Simplicity, yet reliability
- There will be a 10% extra credit for any design that is selected as the best project based on the opinion of an external reviewer.

Course Objectives

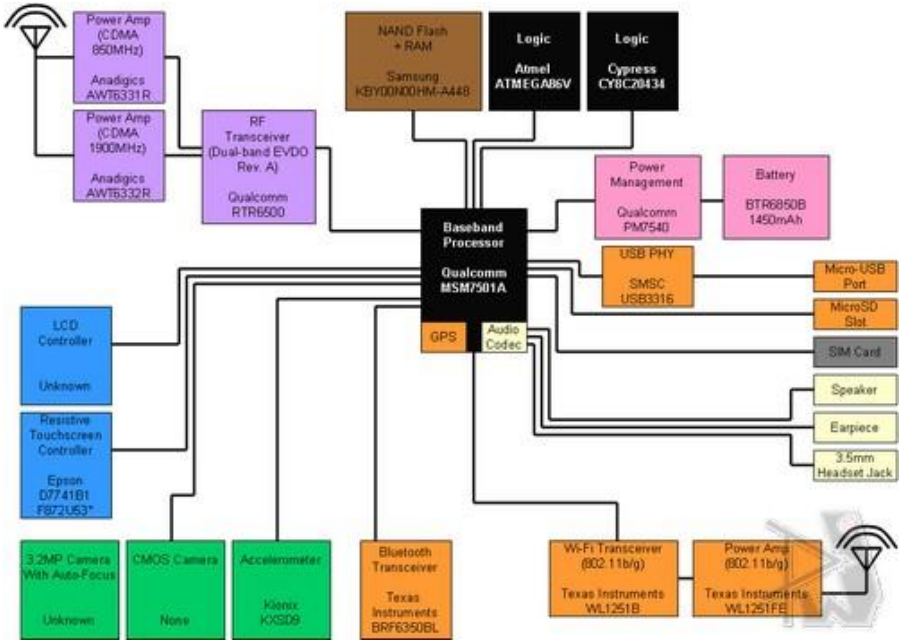
- Design of advanced analog electronic circuits.
- BJT and MOSFET operational amplifiers.
- BJT and MOSFET current mirrors and output stages.
- Frequency response and compensation.
- Feedback and stability.

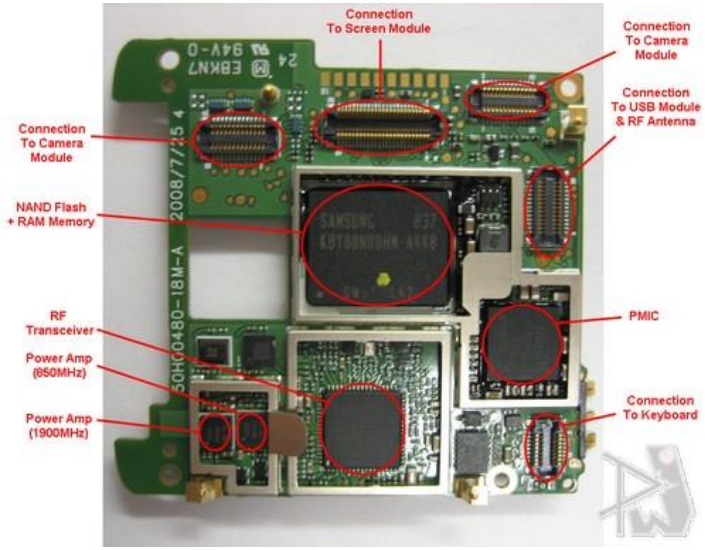
Class Schedule

Warning: Lecture schedule subject to change!!

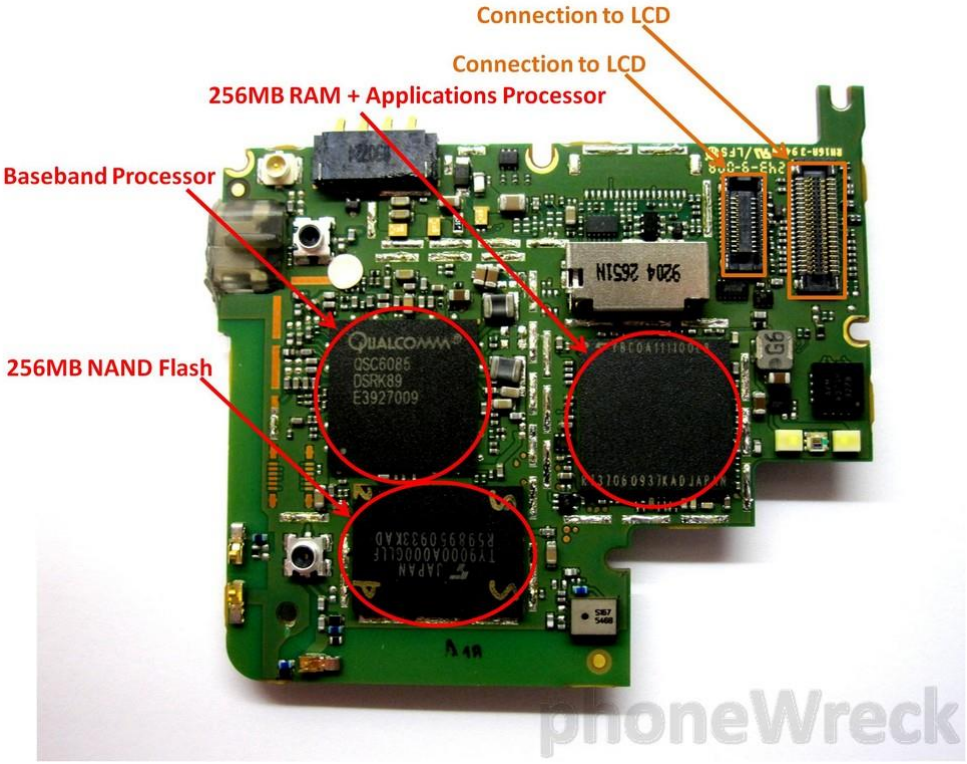
Date	Day	Topic	Reading/Coverage
August 18	Mon	Introduction to Analog Electronics	Handout
August 20	Wed	Review of Basic MOSFET Amplifiers I	5.2 - 5.4
August 25	Mon	Review of Basic MOSFET Amplifiers II	7.1 - 7.5 (CMOS)
August 27	Wed	Review of Basic BJT Amplifiers I	6.2 - 6.4
September 1	Mon	Labor Day	-
September 3	Wed	Review of Basic BJT Amplifiers II	7.1 - 7.5 (BJT)
September 8	Mon	Analog IC Building Blocks: Basic Gain Cells	8.1 - 8.2
September 10	Wed	Analog IC Building Blocks: Cascode Amplifier	8.3
September 15	Mon	Analog IC Building Blocks: Current Sources	8.4
September 17	Wed	Analog IC Building Blocks: Improved Current Mirrors	8.5
September 22	Mon	Analog IC Building Blocks: Transistor Pairings	8.6
September 24	Wed	Differential Amplifiers: MOS Differential Pair	9.1
October 29	Mon	Differential Amplifiers: Small Signal Operation	9.2
October 1	**Wed**	**Midterm Exam #1**	-
October 6	Mon	Differential Amplifiers: BJT Differential Pair	9.3
October 8	Wed	Differential Amplifiers: Nonideal Characteristics	9.4
October 13	Mon	Differential Amplifiers: with Active Loads	9.5 - 9.6
October 15	Wed	Frequency Response: Low-frequency Response	10.1
October 20	Mon	Frequency Response: High-frequency Device Models	10.2
October 22	Wed	Frequency Response: High-frequency Response	10.3
October 27	Mon	Frequency Response: Useful Tools for HF Analysis	10.4.3 & 10.5
October 29	Wed	Frequency Response: Examples (CG & Cascode)	10.6
November 3	Mon	Frequency Response: More Examples	10.9 & 10.10
November 5	**Wed**	**Midterm Exam #2**	-
November 10	Mon	Feedback: Introduction	11.1
November 12	Wed	Feedback: Negative Feedback Properties	11.2
November 17	Mon	Feedback:Stability Analysis using Bode Plots	11.12
November 19	Wed	Feedback: Frequency Compensation	11.13
November 24	Mon	Output Stages: Power Amplifiers	12.1 - 12.6
November 26	Wed	Basic Analog Systems: ADC and DAC Circuits	Handout
December 1	Mon	Op-Amp Design Concepts	13.1 - 13.3
December 3	Wed	Class Final Review	-
December 10	**Wed**	**Final Exam (3:00-5:00PM)**	-

Example of an Analog ICs in HTC Touch Pro

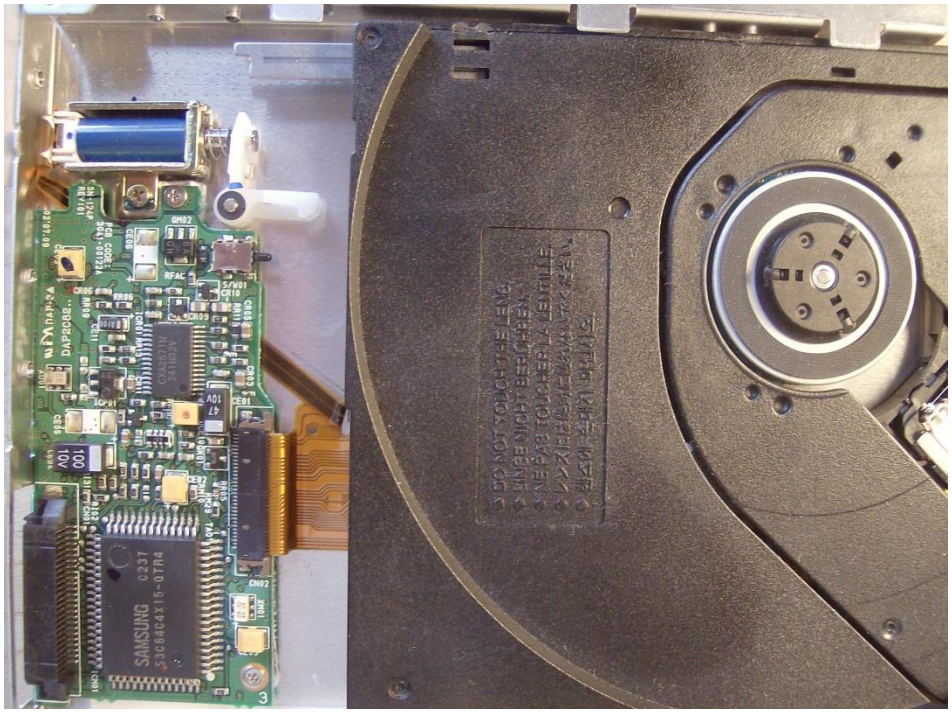




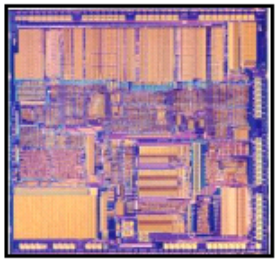
Example of an Analog ICs in Motorola Droid

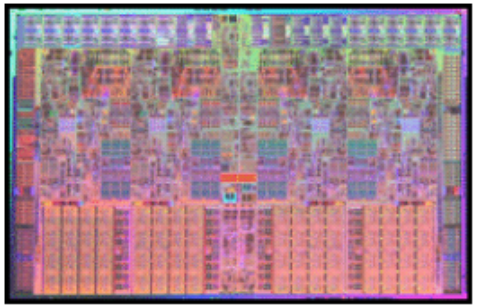


Example of an Analog ICs in a DVD Drive



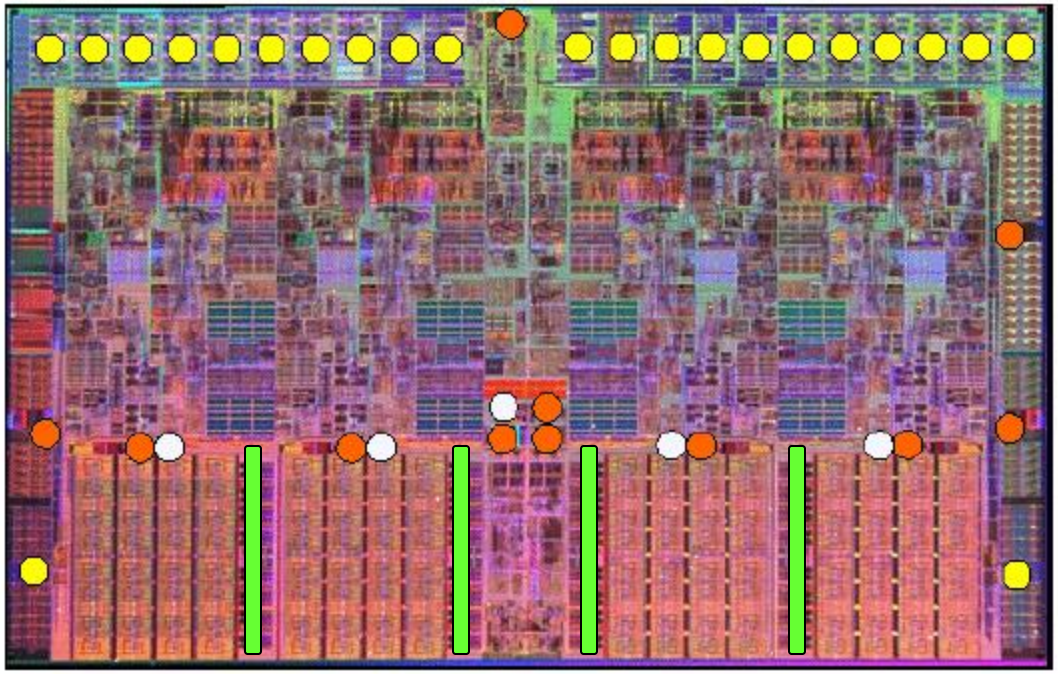
Intel's Microprocessor Evolution





	Intel386™	Nehalem
Transistor Count:	280 thousand	731 million
Frequency:	16 MHz	>3.6 GHz
# Cores:	1	4
Cache Size:	None	8 MB
I/O Peak Bandwidth:	64 MB/sec	50 GB/sec
Adaptive Circuits:	None	Sleep Mode Turbo Mode Power Gating Adaptive Frequency Clocking

Analog Subcircuits in 45nm Nehalem CPU



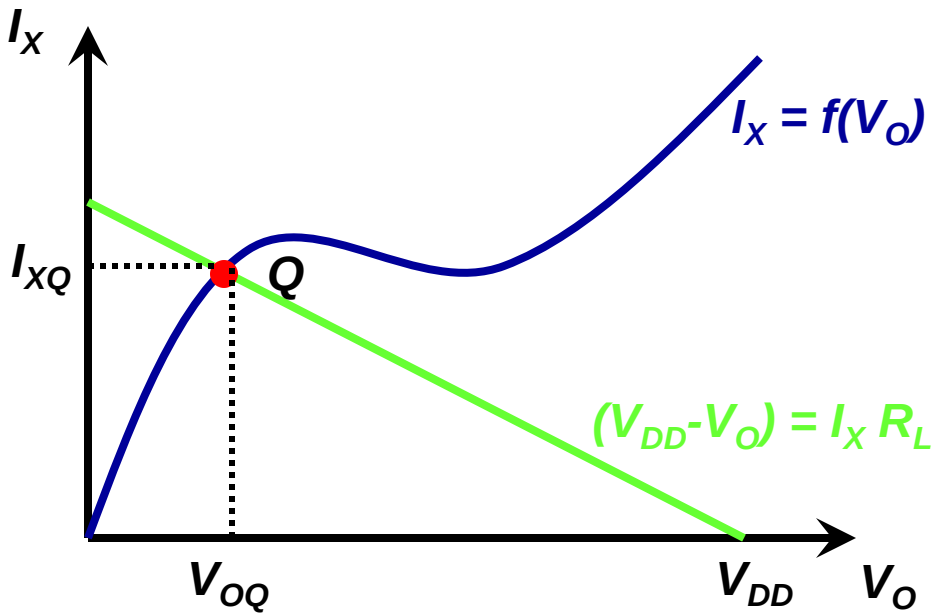
23 master DLL circuits 11 PLL circuits 5 digital thermal sensors

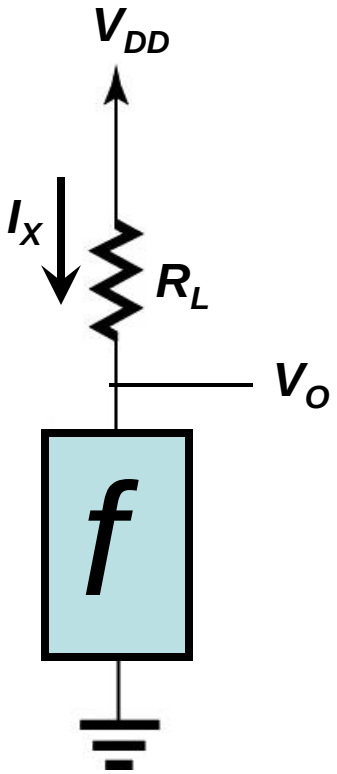
4 arrays of sense amplifiers for cache

Review of MOSFET Amplifiers

- **Concepts of:**
  - **Load Line**
  - **Static Resistance**
  - **Dynamic Resistance**
- **MOSFET I-V Characteristics**
- **MOSFET Circuits at DC**

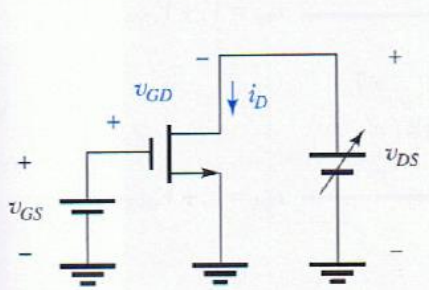
Concept of Load Line, Dynamic and Static R

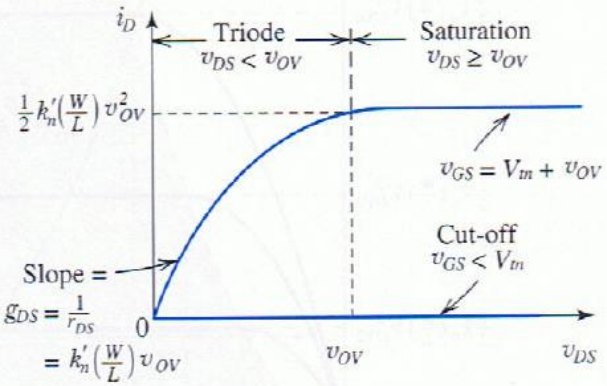




NMOS I-V Characteristics

Table 5.1 Regions of Operation of the Enhancement NMOS Transistor





- $v_{GS} < V_{tn}$: no channel; transistor in cut-off; $i_D = 0$
- $v_{GS} = V_{tn} + v_{OV}$: a channel is induced; transistor operates in the triode region or the saturation region depending on whether the channel is continuous or pinched-off at the drain end;

Triode Region

Continuous channel, obtained by:

$$v_{GD} > V_{tn}$$

or equivalently:

$$v_{DS} < v_{OV}$$

Then,

$$i_D = k_n'\left(\frac{W}{L}\right)\left[(v_{GS} - V_{tn})v_{DS} - \frac{1}{2}v_{DS}^2\right]$$

or equivalently,

$$i_D = k_n'\left(\frac{W}{L}\right)\left(v_{OV} - \frac{1}{2}v_{DS}\right)v_{DS}$$

Saturation Region

Pinched-off channel, obtained by:

$$v_{GD} \leq V_{tn}$$

or equivalently:

$$v_{DS} \geq v_{OV}$$

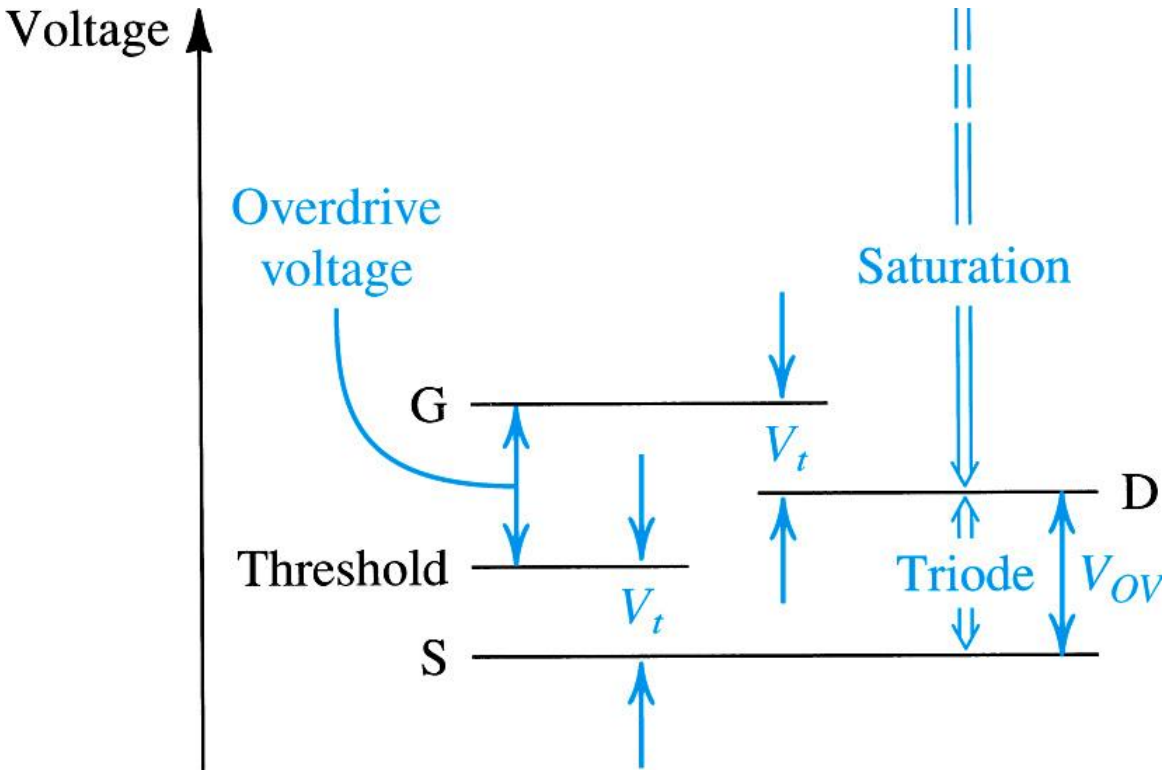
Then

$$i_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)(v_{GS} - V_{tn})^2$$

or equivalently,

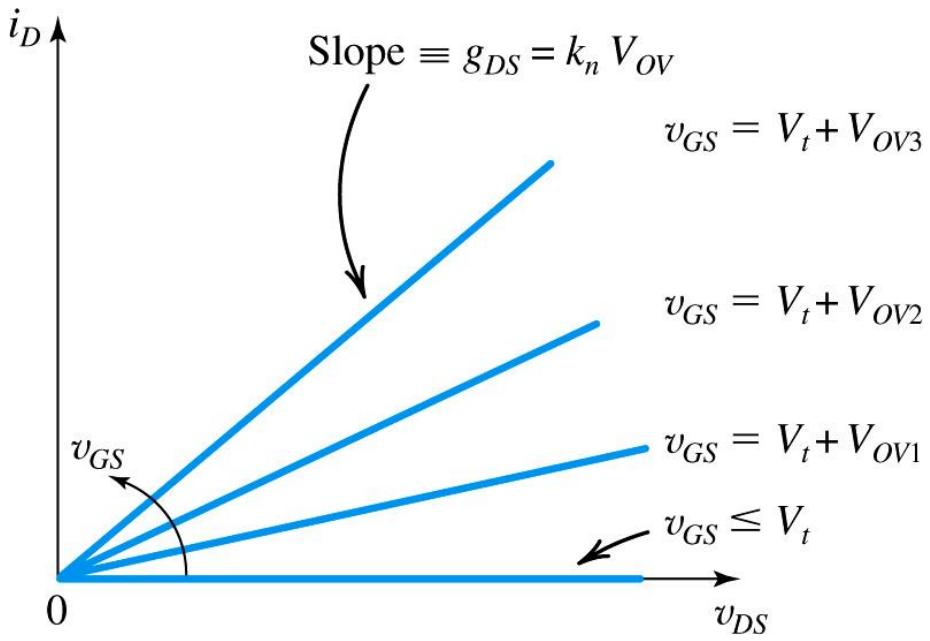
$$i_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)v_{OV}^2$$

Concept of V_{OV} and V_{DS-MIN} in NMOS



How about PMOS?

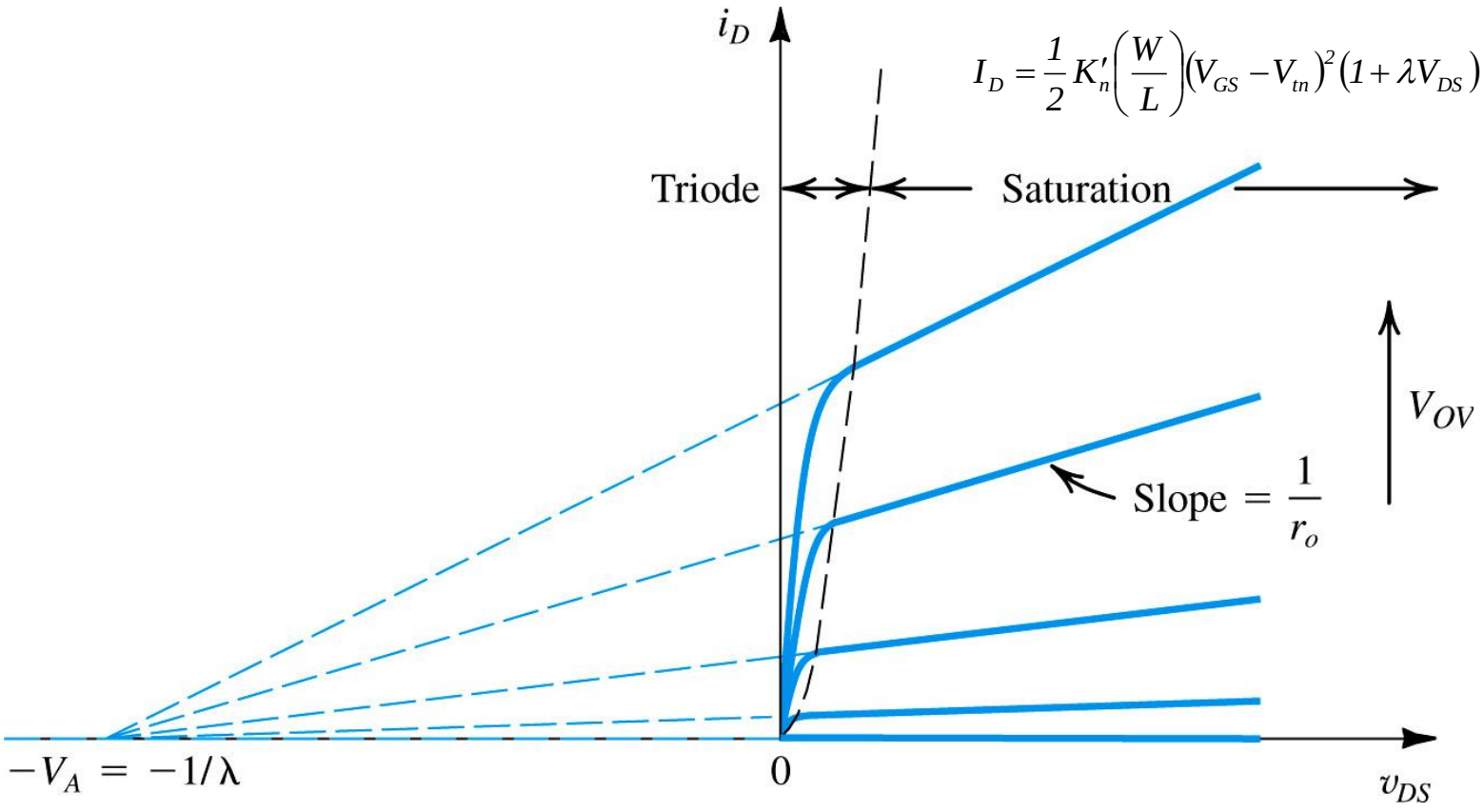
Dynamic D/S Resistance in Triode Region



D/S Resistance in Triode Region:

$$r_{DS} = \frac{1}{K_n'\left(\frac{W}{L}\right)\left(V_{GS} - V_t\right)}$$

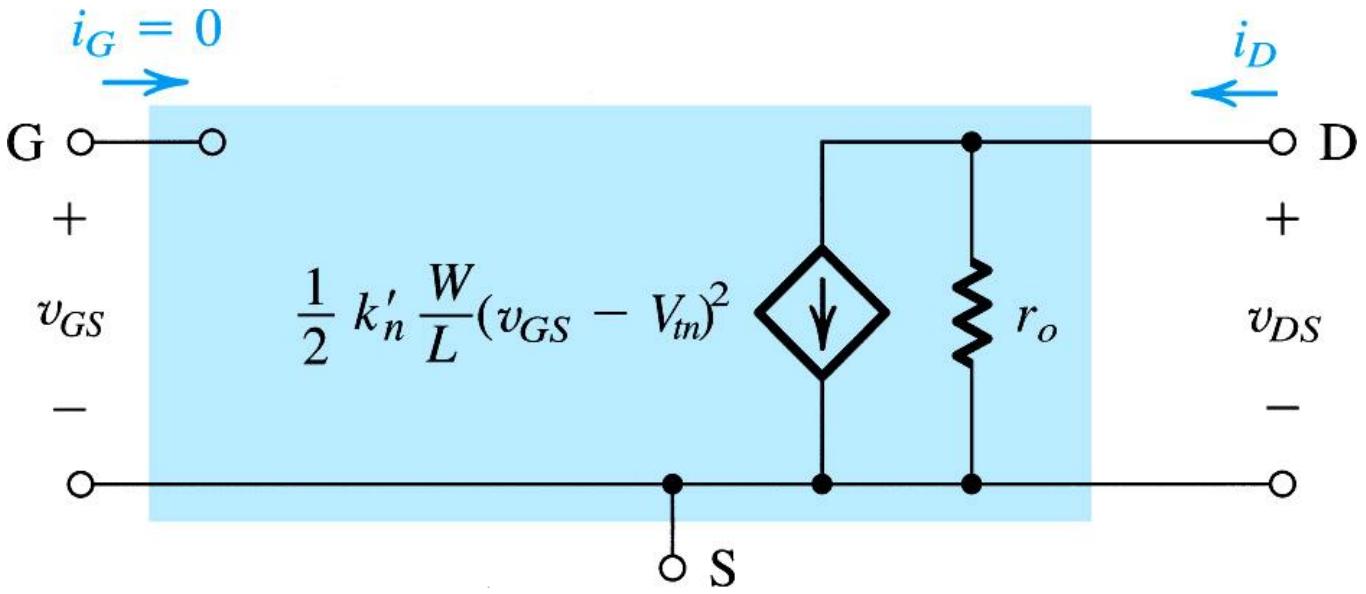
Channel Length Modulation Effect



1) $r_o = \dfrac{1}{\lambda I_D} = \dfrac{V_A}{I_D}$

2) $V_A \propto L \quad \Rightarrow \quad r_o \propto L$

Large Signal MOSFET Model in Saturation



Output Resistance in Saturation: $$r_o = \frac{1}{\lambda I_D} = \frac{V_A}{I_D}$$

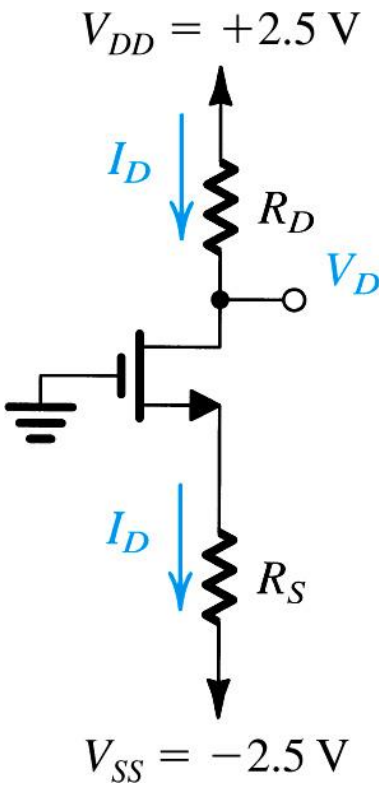
Notes:

1) For DC analysis, we normally assume λ≈0.

2) It is easier to think of overdrive voltages for DC analysis.

MOSFET Circuits at DC: Example 1

Design the following circuit, so that the transistor operates at I_D = 0.4 mA and V_D = +0.5 V. The NMOS transistor has V_t = 0.7 V, K'_n = 100 µA/V^2, L = 1 µm, and W = 32 µm. Neglect the channel-length modulation effect.



MOSFET Circuits at DC: Example 2

D5.9 For the circuit in Fig. E5.9, find the value of R that results in $V_D = 0.8$ V. The MOSFET has $V_{tn} = 0.5$ V, $\mu_n C_{ox} = 0.4$ mA/V^2, $W/L = \frac{0.72\ \mu m}{0.18\ \mu m}$, and $\lambda = 0$.

Ans. 13.9 kΩ

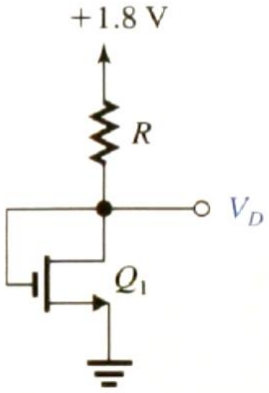


Figure E5.9

D5.10 Figure E5.10, shows a circuit obtained by augmenting the circuit of Fig. E5.9 considered in Exercise 5.9 with a transistor Q_2 identical to Q_1 and a resistance R_2. Find the value of R_2 that results in Q_2 operating at the edge of the saturation region. Use your solution to Exercise 5.9.

Ans. 20.8 kΩ

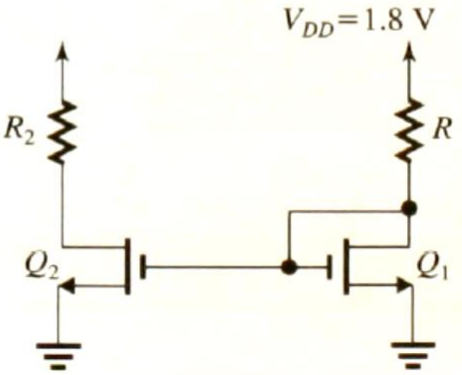
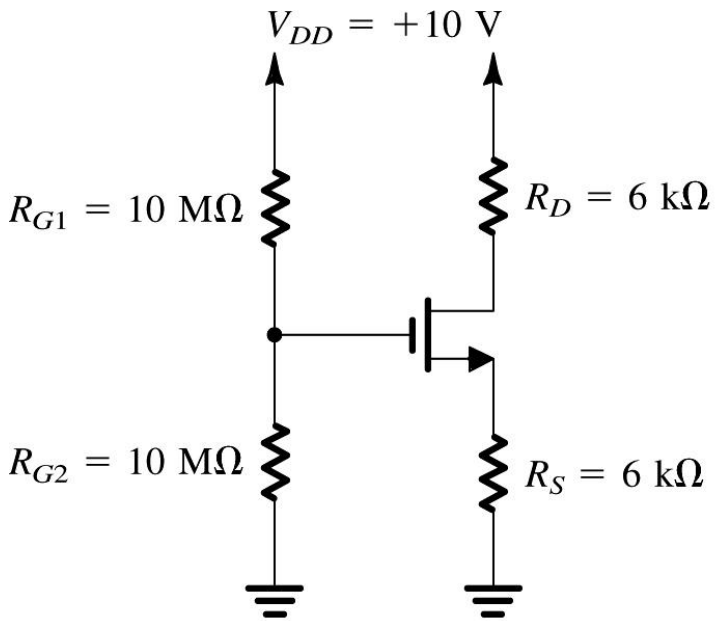


Figure E5.10

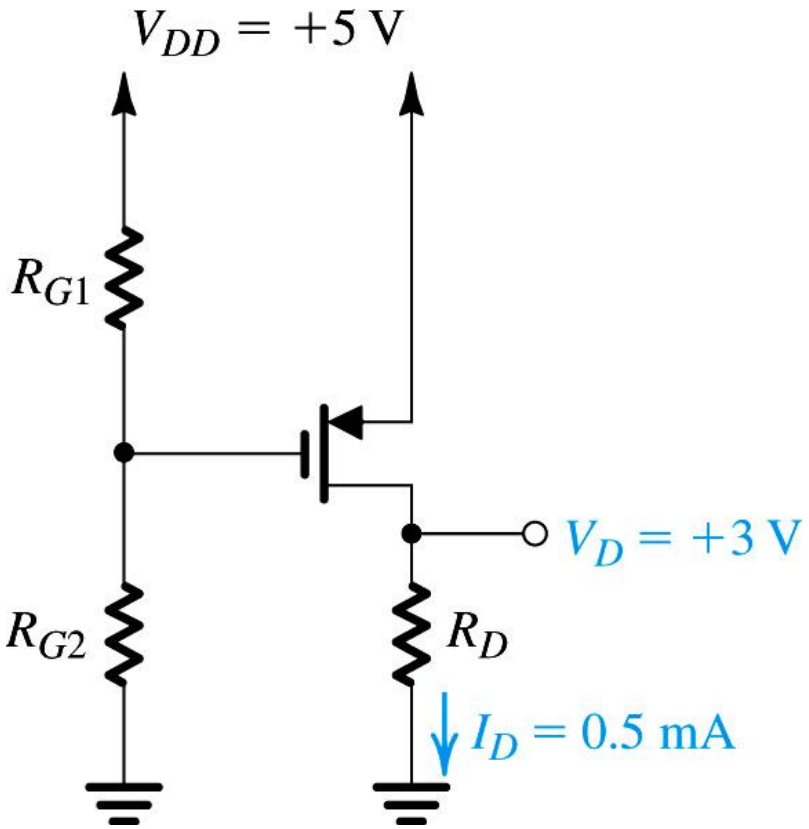
MOSFET Circuits at DC: Example 3

Analyze the circuit shown below to determine the voltages at all nodes and the currents through all branches. Let V_{tn} = 1 V and $K'_n(W/L)$ = 1 mA/V^2
What is the largest value that R_D can have while the transistor remains in the saturation mode.



MOSFET Circuits at DC: Example 4

Design the circuit shown below so that the transistor operates in saturation with I_D=0.5mA and V_D=+3V. Let V_{tp} = -1 V and $K'_p(W/L)$ = 1 mA/V^2
What is the largest value that R_D can have while the transistor remains in the saturation mode?



MOSFET Circuits at DC: Example 5

For the circuit below, find the value of R that results in the PMOS transistor operating with an overdrive voltage $|V_{OV}| = 0.6$ V. The threshold voltage is $V_{tp} = -0.4$ V, the process tranconductance parameter $K'_p = 0.1$ mA/V^2 and W/L=10µm/0.18µm.