

ECE 523/421 – Analog Electronics

Lecture 2: Basic MOSFET Amplifiers I

Payman Zarkesh-Ha

Office: ECE Bldg. 230B

Office hours: Tuesday 2:00-3:00PM or by appointment

E-mail: pzarkesh@unm.edu

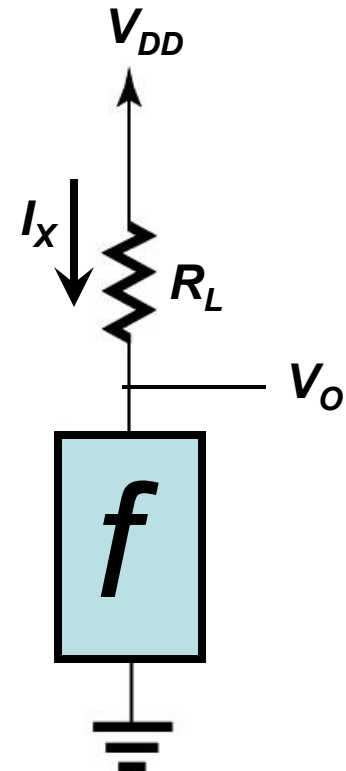
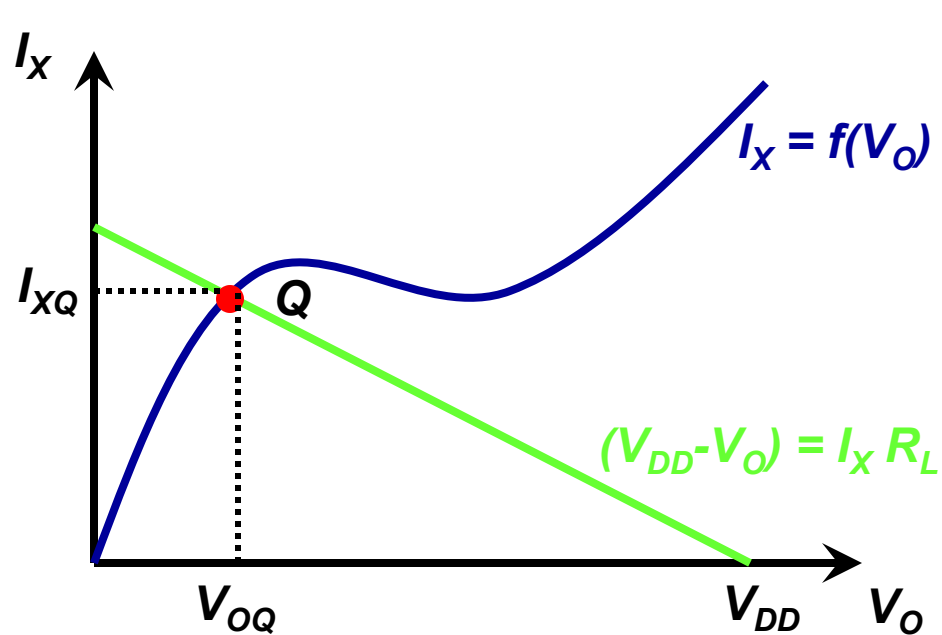
Review of Last Lecture

- ☐ **MOSFET I-V Characteristics**
- ☐ **MOSFET Circuits at DC**

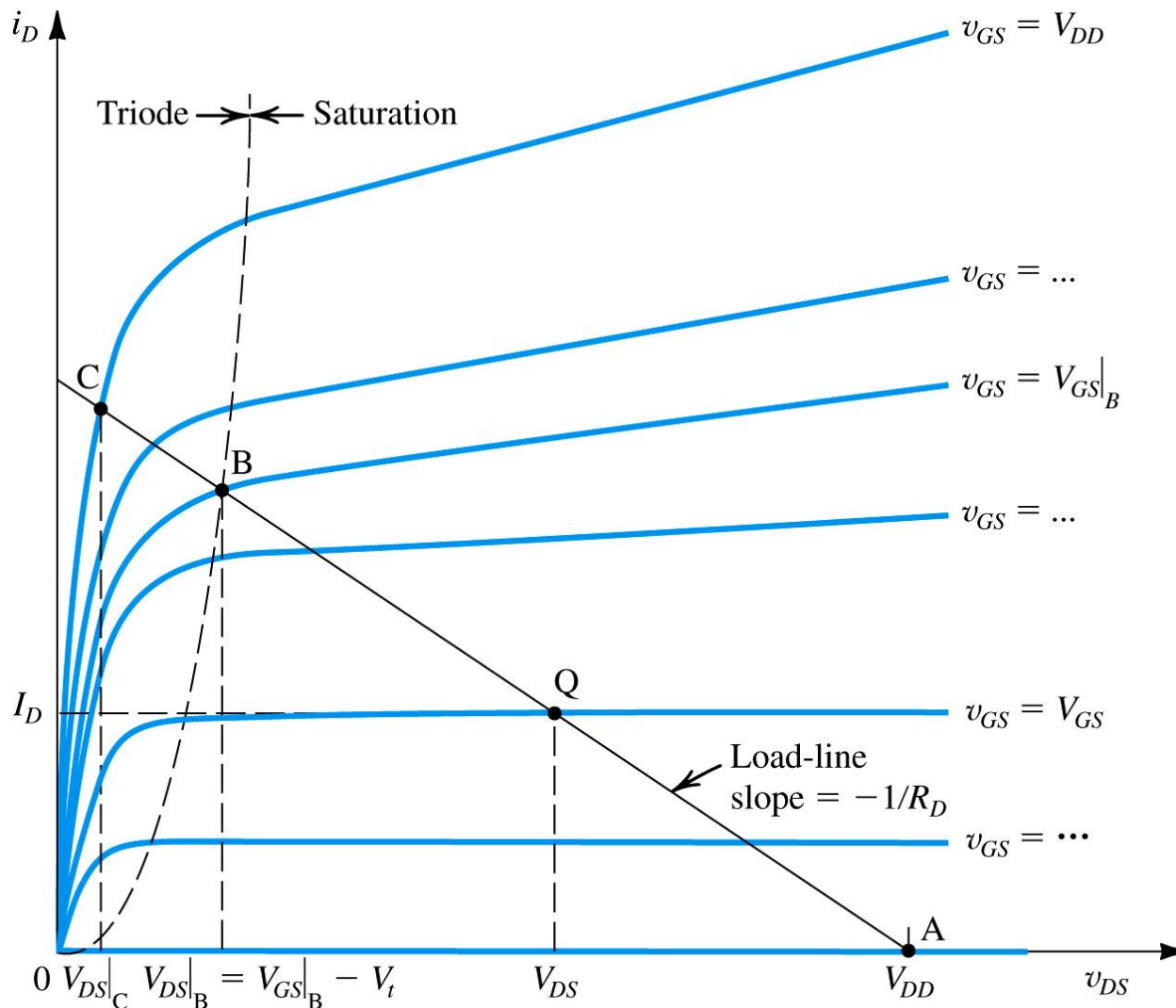
Today's Lecture

- ☐ **Concepts of:**
 - **Load Line**
 - **Static Resistance**
 - **Dynamic Resistance**
- ☐ **MOSFET Biasing for Amplification**
- ☐ **MOSFET Small Signal (Π and T Models)**
- ☐ **Basic MOSFET Amplifier Configurations (CS, CG, CD)**
- ☐ **Examples**

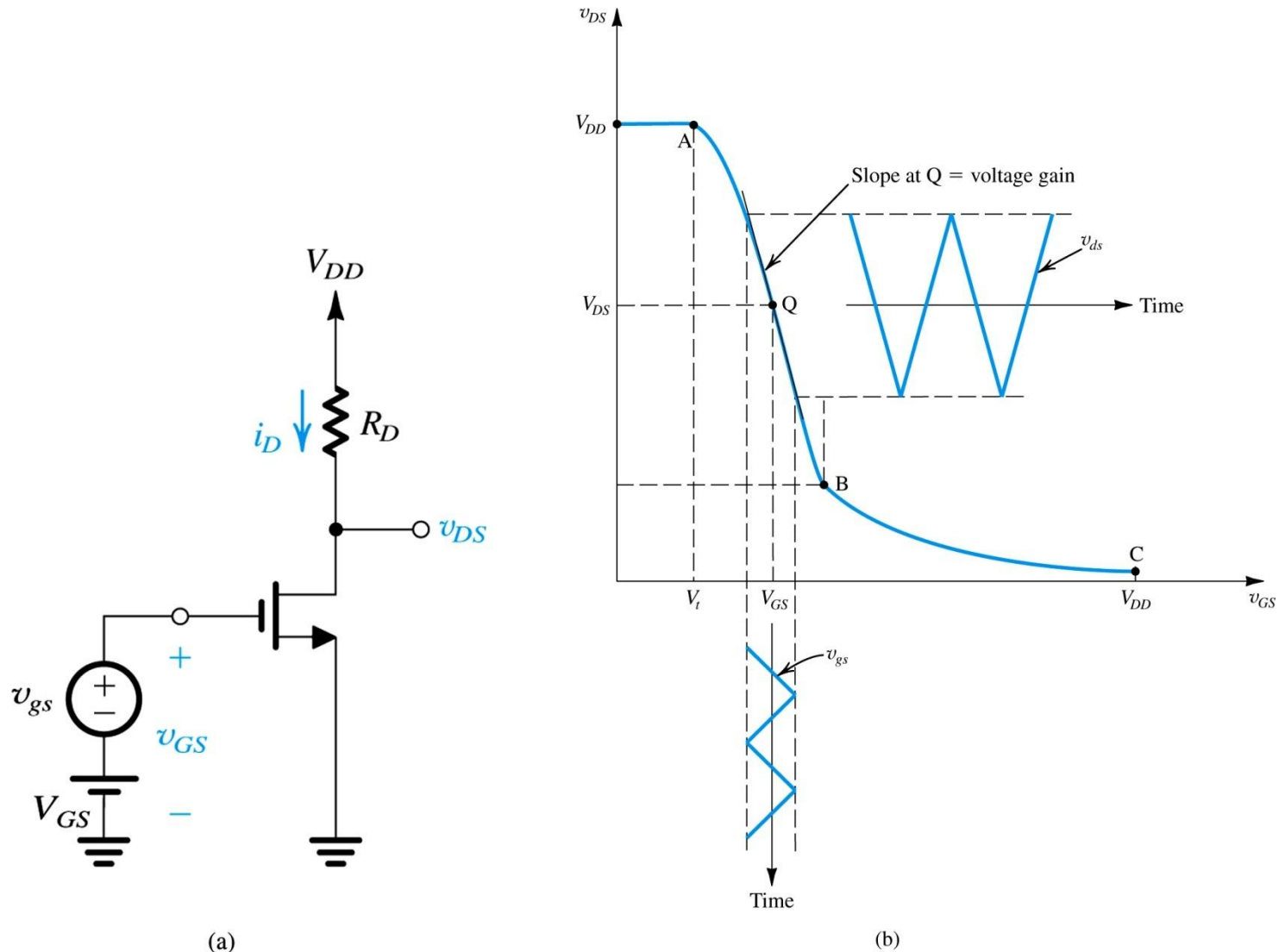
Concept of Load Line, Dynamic and Static R



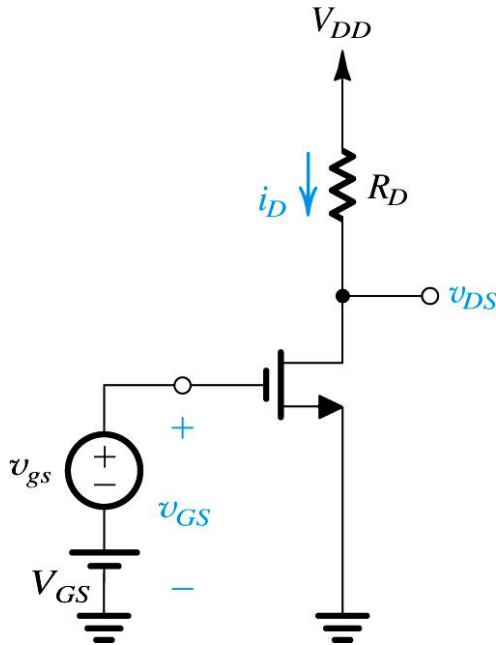
Choosing The Right Q-Point



Voltage Transfer Characteristics (VTC)



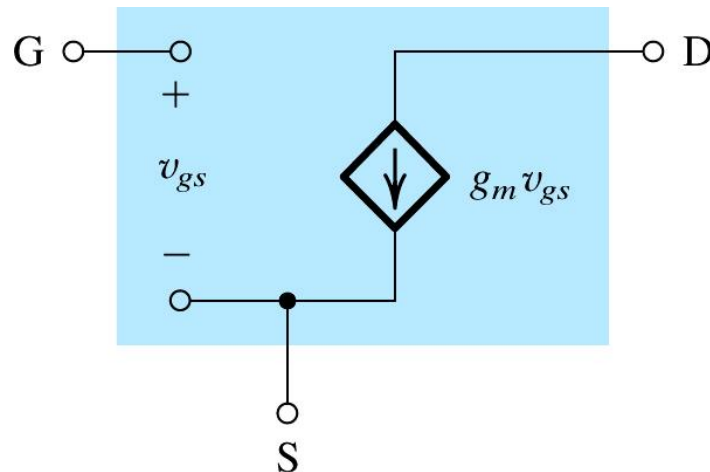
Basic Amplification Equations



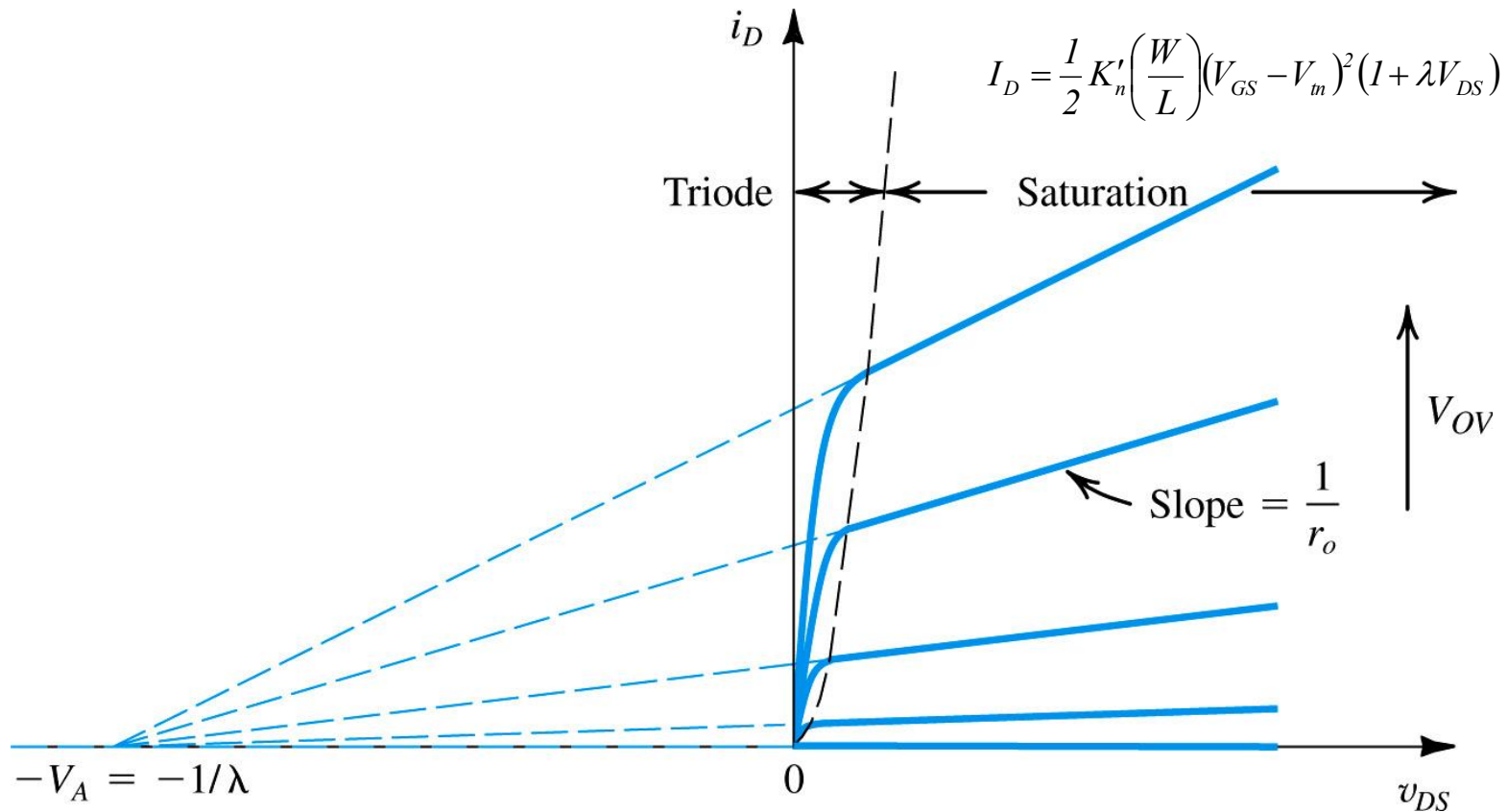
$$i_D = \frac{K'_n}{2} \left(\frac{W}{L} \right) (V_{GS} + v_{gs} - V_{tn})^2$$

$$i_D \approx \underbrace{\frac{K'_n}{2} \left(\frac{W}{L} \right) (V_{GS} - V_{tn})^2}_{\text{DC Portion}} + \underbrace{K'_n \left(\frac{W}{L} \right) (V_{GS} - V_{tn}) v_{gs}}_{\text{AC Portion}}$$

$\nearrow g_m$



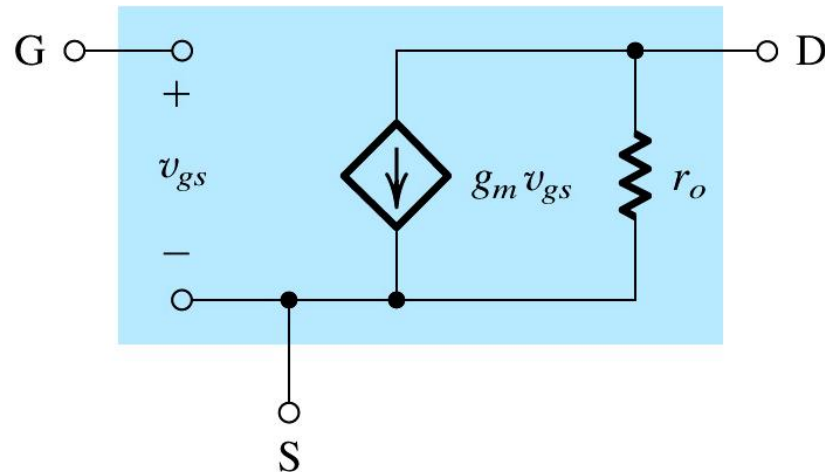
Channel Length Modulation Effect



$$1) \quad r_o = \frac{1}{\lambda I_D} = \frac{V_A}{I_D}$$

$$2) \quad V_A \propto L \Rightarrow r_o \propto L$$

MOSFET Small Signal Equivalent Circuit

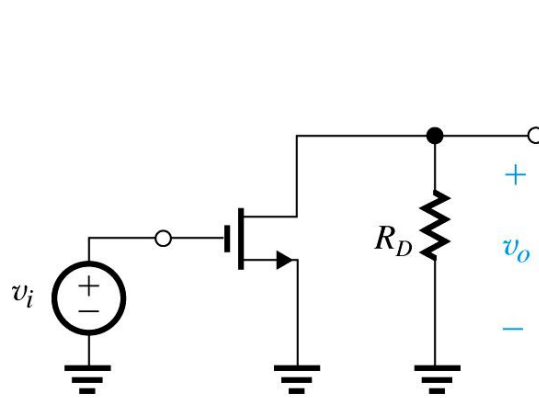


Where:

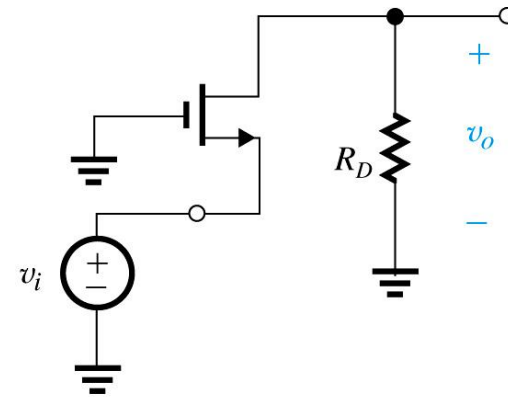
$$g_m = K'_n \left(\frac{W}{L} \right) V_{OV} = \frac{2I_D}{V_{OV}} = \sqrt{2K'_n \left(\frac{W}{L} \right) I_D}$$

$$r_o = \frac{1}{\lambda I_D} = \frac{|V_A|}{I_D}$$

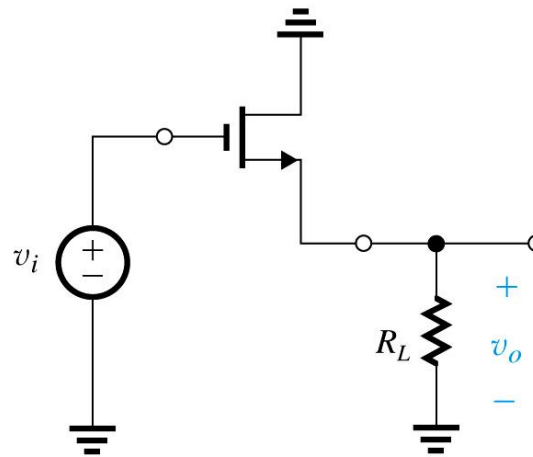
Basic MOFET Amplifier Configurations



(a) Common Source (CS)

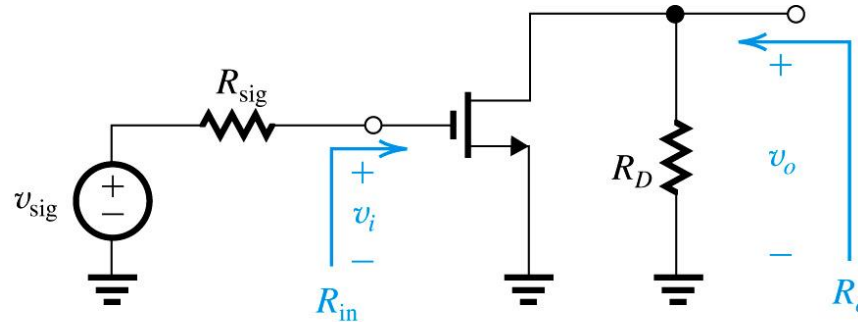


(b) Common Gate (CG)



(c) Common Drain (CD)

Common Source (CS) Amplifier



$$R_{in} = \infty$$

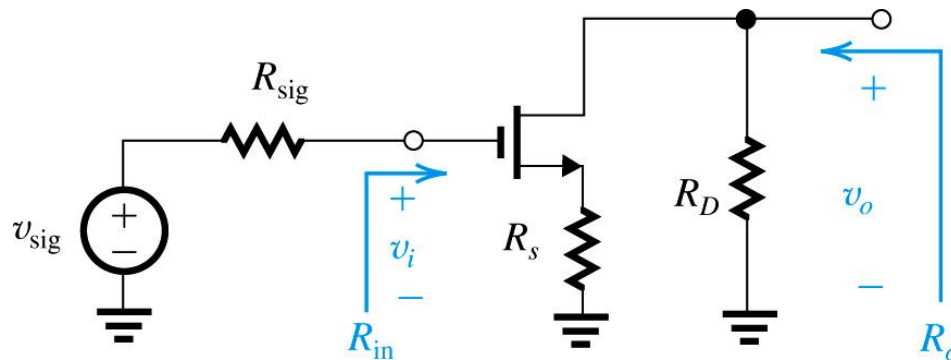
$$R_o = R_D \parallel r_o$$

$$A_v = \frac{v_o}{v_i} = -g_m (R_D \parallel r_o)$$

$$G_v = \frac{v_o}{v_{sig}} = -g_m (R_D \parallel r_o)$$

- ☐ Infinite input resistance
- ☒ Large gain
- ☐ Sensitive bias
- ☐ Large output resistance
- ☐ Limited bandwidth

CS Amplifier with Source-Degeneration Res.



$$R_{in} = \infty$$

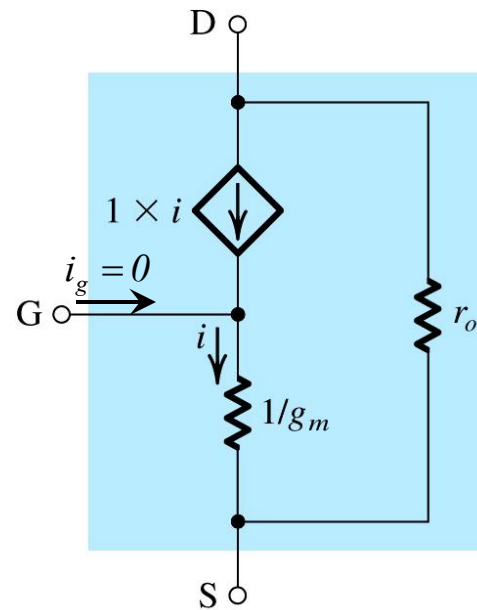
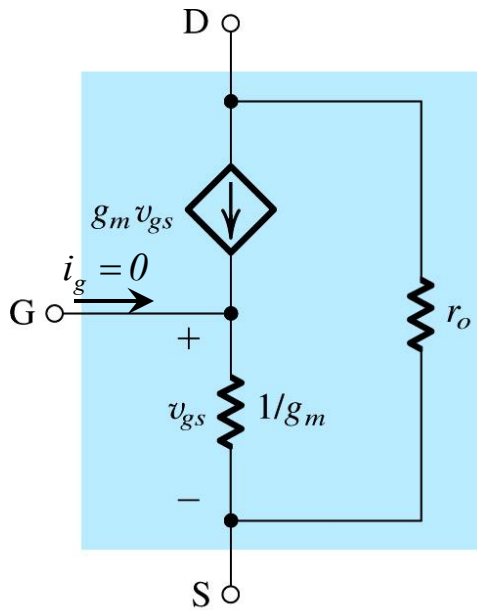
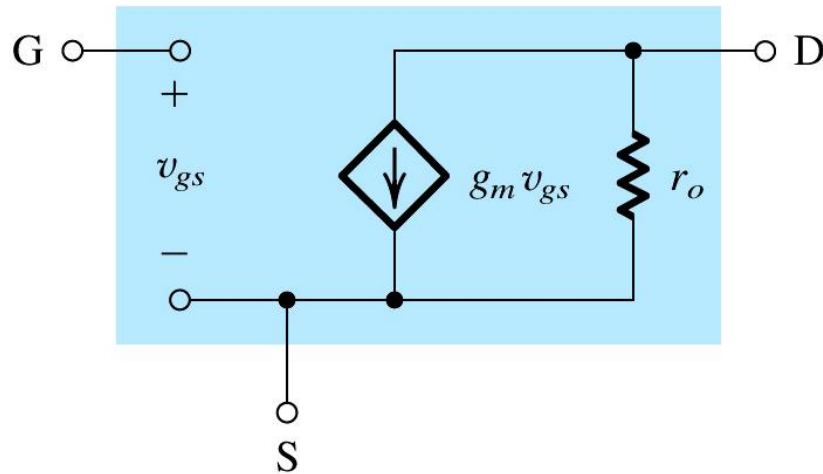
$$R_o \approx R_D \parallel ((1 + g_m R_s) r_o)$$

$$A_v = \frac{v_o}{v_i} \approx -\frac{g_m}{1 + g_m R_s} [R_D \parallel ((1 + g_m R_s) r_o)]$$

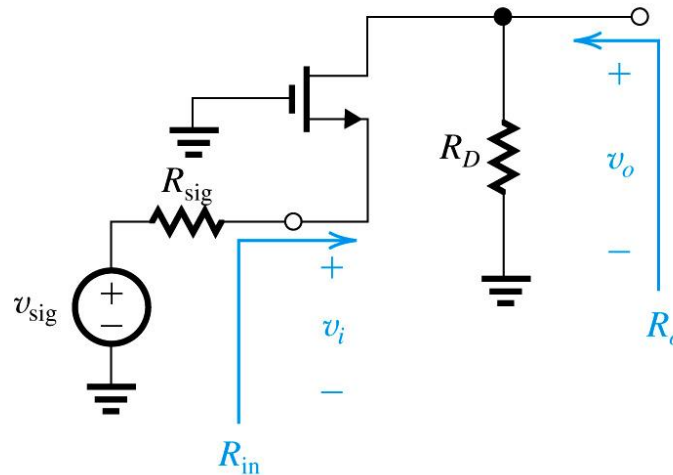
$$G_v = \frac{v_o}{v_{sig}} = \frac{v_o}{v_i} = A_v$$

- ☐ Infinite input resistance
- ☐ Less sensitive bias
- ☐ Better bandwidth
- ☐ Degenerated gain
- ☐ Large output resistance

MOSFET Small Signal T Model



Common Gate (CG) Amplifier



$$R_{in} \approx \frac{1}{g_m} + \frac{R_D}{1 + g_m r_o}$$

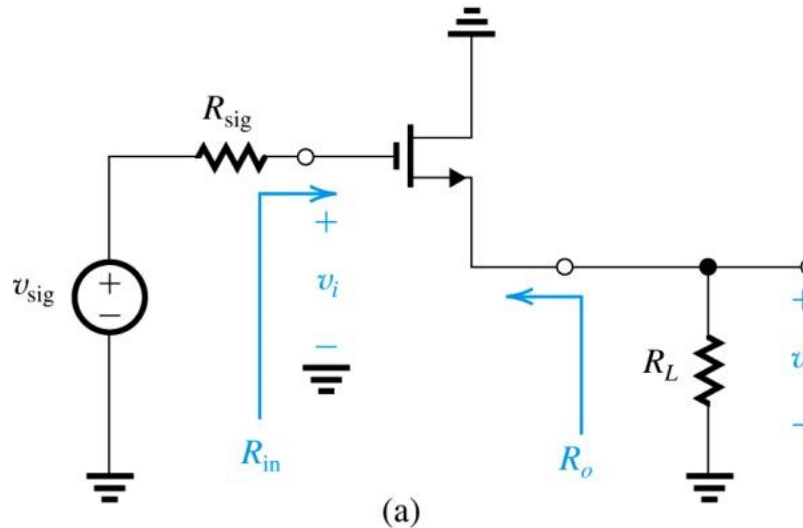
$$R_o = R_D \parallel r_o$$

$$A_v = \frac{v_o}{v_i} = \frac{R_D}{R_{in}}$$

$$G_v = \frac{v_o}{v_{sig}} = \frac{R_D}{R_{sig} + R_{in}}$$

- ☐ Low input resistance
- ☐ High bandwidth
- ☐ Small gain
- ☐ Large output resistance

Common Drain (CD) Amplifier



$$R_{in} = \infty$$

$$R_o \approx \frac{1}{g_m}$$

$$A_v = \frac{v_o}{v_i} = \frac{R_L}{R_L + 1/g_m}$$

$$G_v = \frac{v_o}{v_{sig}} = \frac{v_o}{v_i} = A_v$$

- ❑ Infinite input resistance
- ❑ Very high bandwidth
- ❑ Unity gain
- ❑ Low output resistance

Example 1: CS Amplifier

- 1) A CS amplifier utilizes a MOSFET biased at $I_D = 0.25$ mA With $V_{OV} = 0.25$ V and $R_D = 20$ K Ω . The device has $V_A = 50$ V. The amplifier is fed with a source having $R_{sig} = 100$ K Ω , and a 20K Ω load is connected to the output Find R_{in} , A_v , R_o and G_v . If to maintain reasonable linearity, the peak of the input sine-wave signal is limited to 10% of $(2V_{OV})$, what is the peak of the sine-wave voltage at the output?
- 2) In the previous circuit, we applied an input signal , v_{sig} of 50 mV peak and obtained an output signal of approximately 1 V peak. Assume that for some reason we now have an Input signal v_{sig} that is 0.2V peak and that we wish to modify the circuit to keep v_{gs} unchanged, and thus keep the nonlinear distortion from increasing. What value should we use for R_s ? What value of G_v Will result? What will the peak signal at the output become?

Example 2: CG Amplifier

- 1) A CG amplifier is required to match a signal source with $R_{\text{sig}} = 100 \, \Omega$. At what current I_D should the MOSFET be biased if it is operated at an overdrive voltage of 0.20 V? If the total resistance in the drain circuit is 2 k Ω , what overall voltage gain is realized?

Example 3: Source Follower

- 1) It is required to design a source follower with $R_o=100\Omega$, $R_L=1K\Omega$, and $V_{in}=1V$. If the MOSFET is operated with an overdrive voltage $V_{OV} = 0.25 V$, at what drain current should it be biased? Find the output Signal amplitude and the signal amplitude between gate and source.

- 2) A MOSFET is connected in the source-follower configuration and employed as the output stage of a cascade amplifier. It is required to provide an output resistance of 200Ω . If the MOSFET has $k'_n = 0.4 \text{ mA/V}^2$ and is operated at $V_{OV} = 0.25 V$, find the required W/L ratio. Also specify the dc bias current I_D . If the amplifier load resistance varies over the range $1k\Omega$ to $10 k\Omega$, what is the range of G_v of the source follower?