ECE 523/421 – Analog Electronics

Lecture 27: Basic Analog Systems: ADC and DAC

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Review of Last Lecture

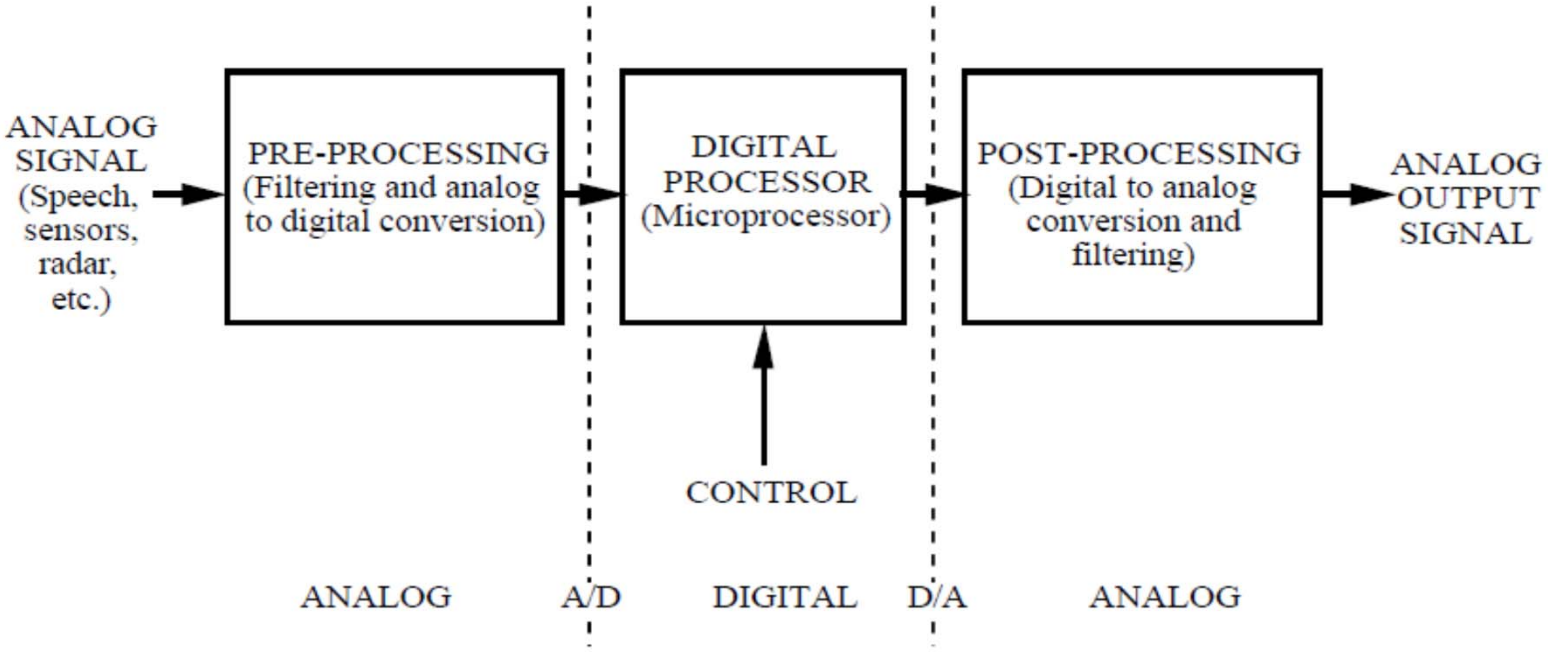
- **Review of Class A Power Amplifier**
- **Class B and Class AB Power Amplifiers**

Today's Lecture

- **Basic Digital to Analog Converters**
- **Basic Analog to Digital Converters**

Courtesy of Prof. Philip Allen

Importance of Data Conversion



Courtesy of Prof. Philip Allen

Digital-to-Analog Converters

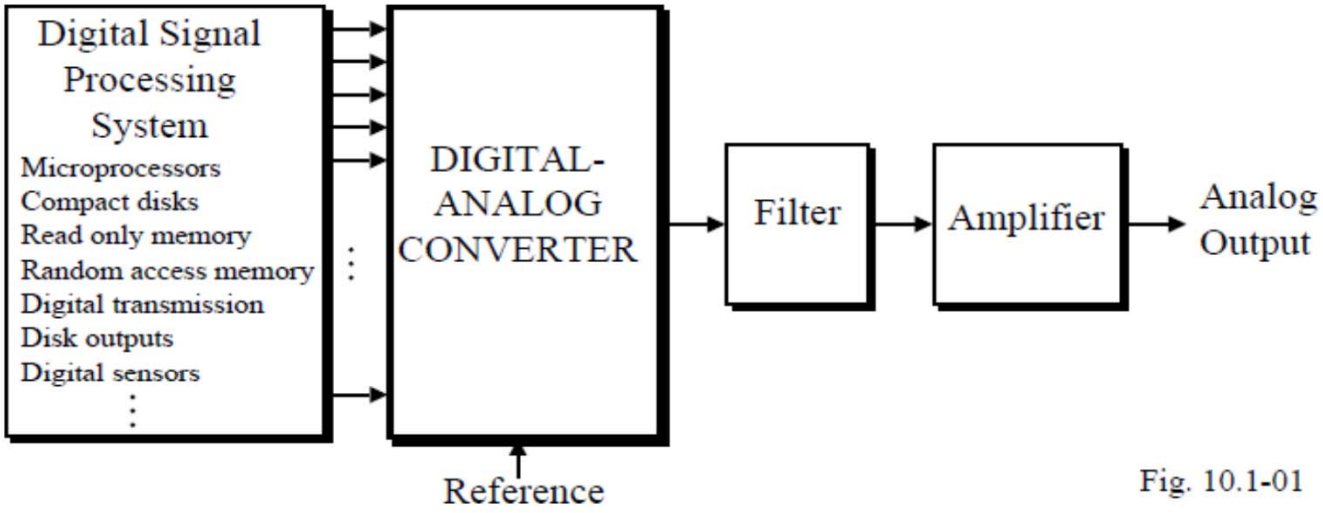


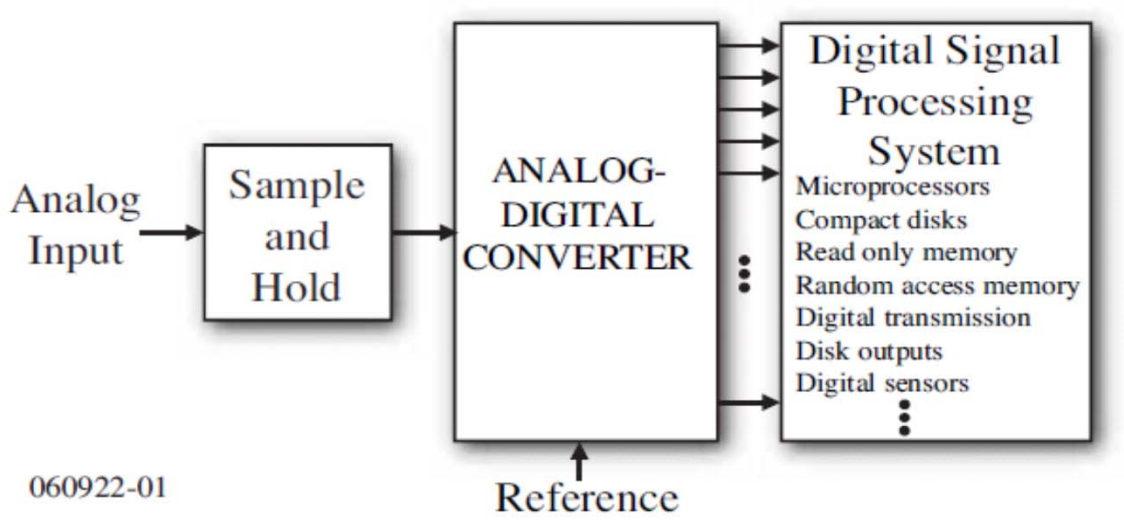
Fig. 10.1-01

Characteristics:

- Can be asynchronous or synchronous
- Primary active element is the op amp
- Conversion time can vary from fast (one clock period, T) to slow ($2^{\text{No. of bits}} * T$)

Courtesy of Prof. Philip Allen

Analog-to-Digital Converters



Characteristics:

- Can only be synchronous (the analog signal must be sampled and held during conversion)
- Primary active element is the comparator
- Conversion time can vary from fast (one clock period, T) to slow ($2^{\text{No. of bits}} * T$)

Courtesy of Prof. Philip Allen

Digital-to-Analog Block Diagram

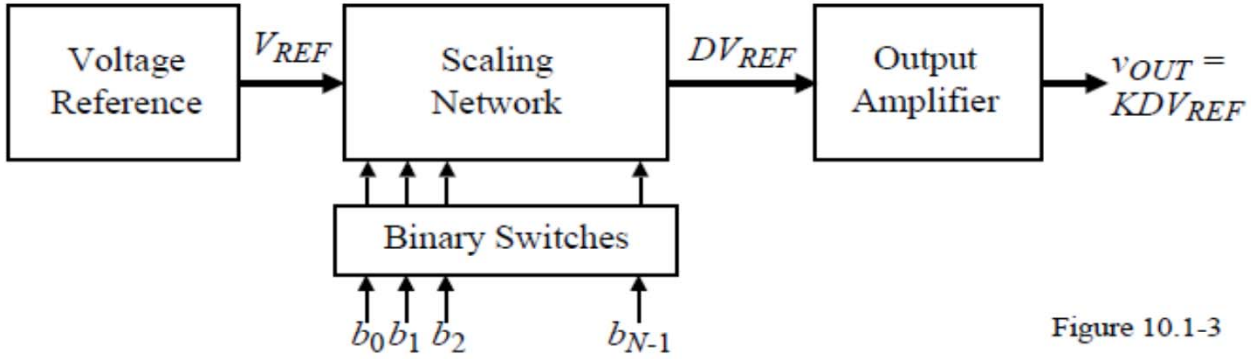


Figure 10.1-3

b_0 is the most significant bit (MSB)

The MSB is the bit that has the most (largest) influence on the analog output

b_{N-1} is the least significant bit (LSB)

The LSB is the bit that has the least (smallest) influence on the analog output

Courtesy of Prof. Philip Allen

Current Scaling DAC

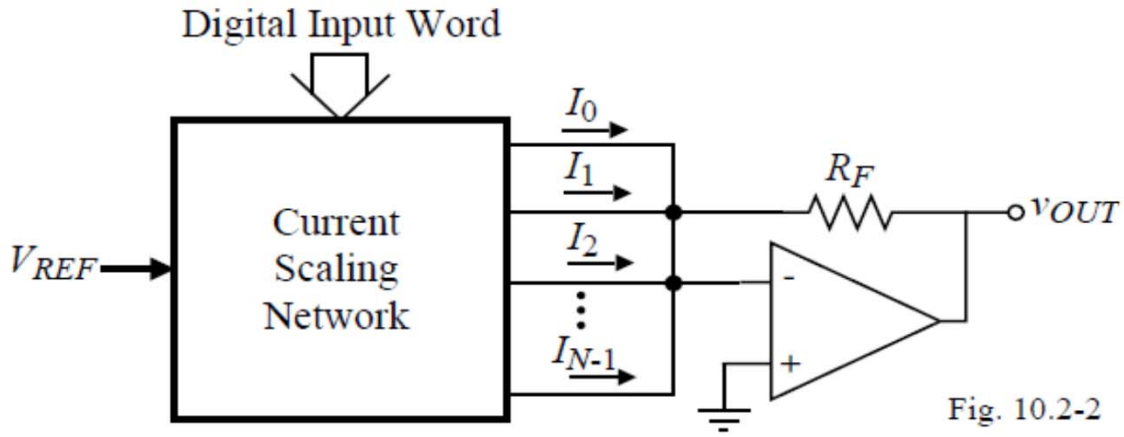


Fig. 10.2-2

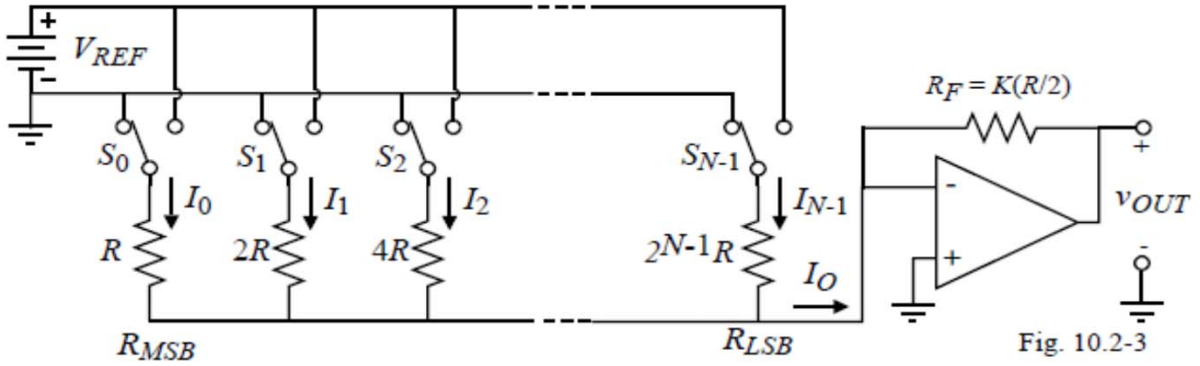


Fig. 10.2-3

Courtesy of Prof. Philip Allen

R-2R Ladder Implementation

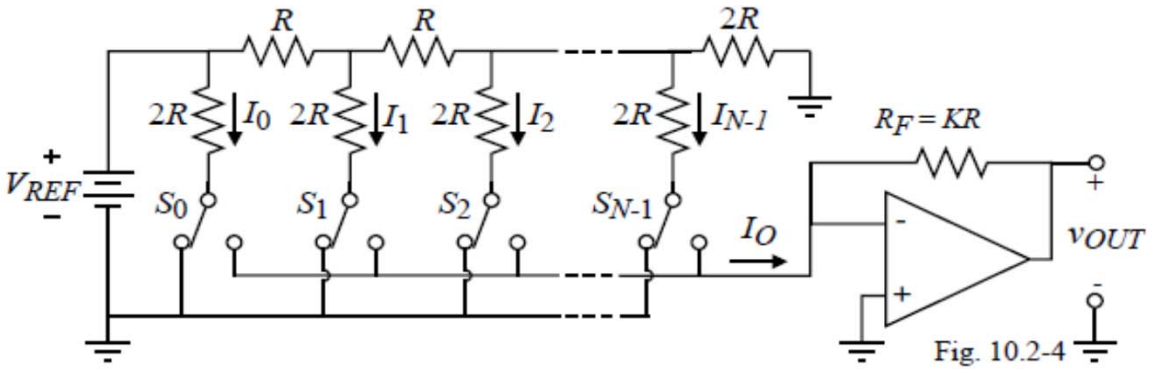


Fig. 10.2-4

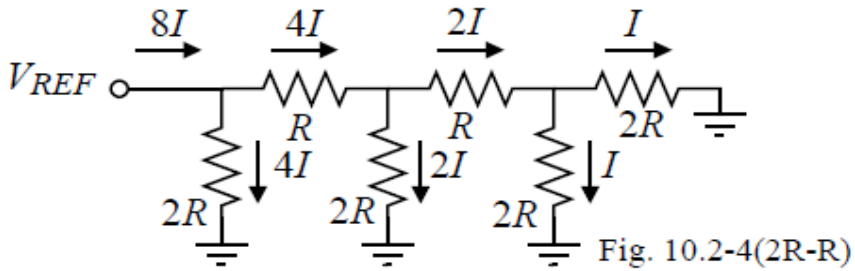


Fig. 10.2-4(2R-R)

Courtesy of Prof. Philip Allen

Current Scaling by Weighted MOSFET

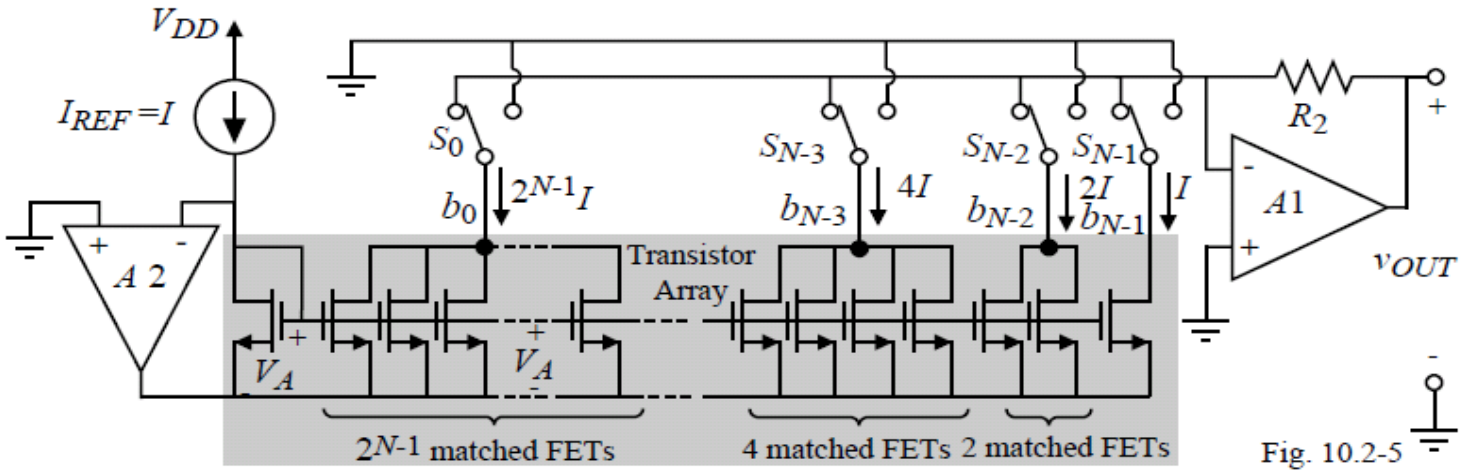
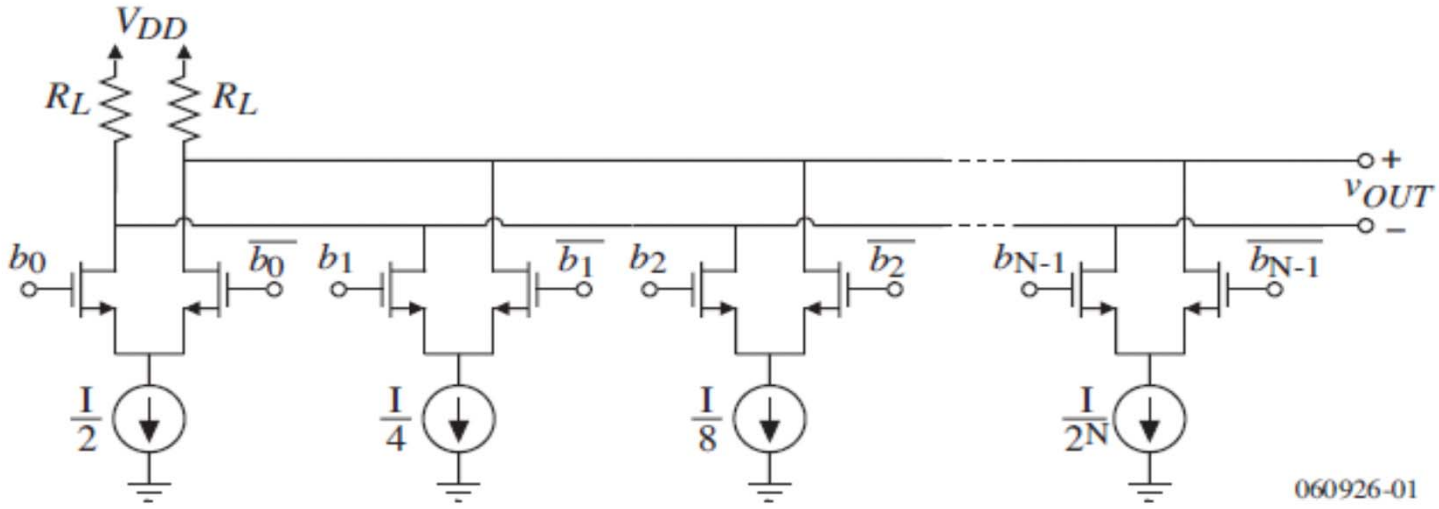


Fig. 10.2-5

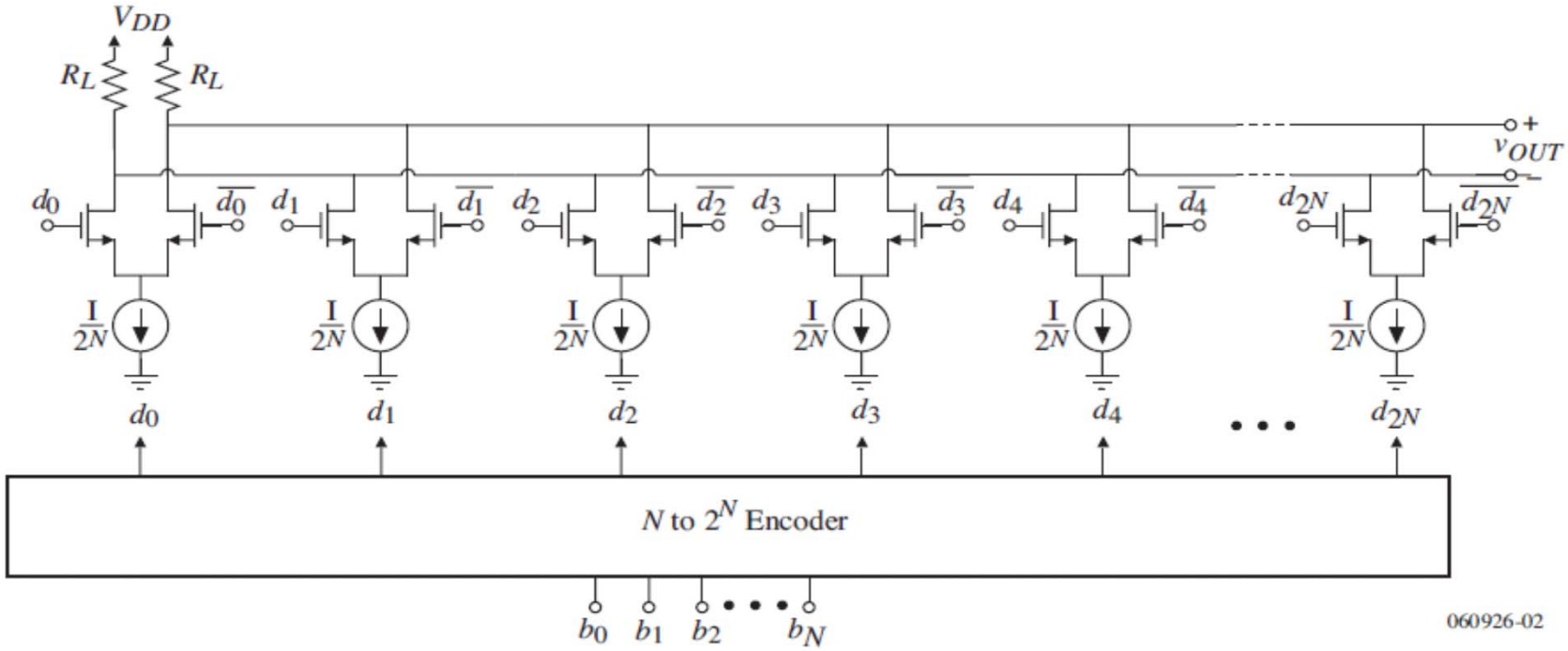
Courtesy of Prof. Philip Allen

High Speed Current-Mode DAC



Courtesy of Prof. Philip Allen

High-Speed, High-Accuracy DAC



Courtesy of Prof. Philip Allen

Voltage Scaling DAC

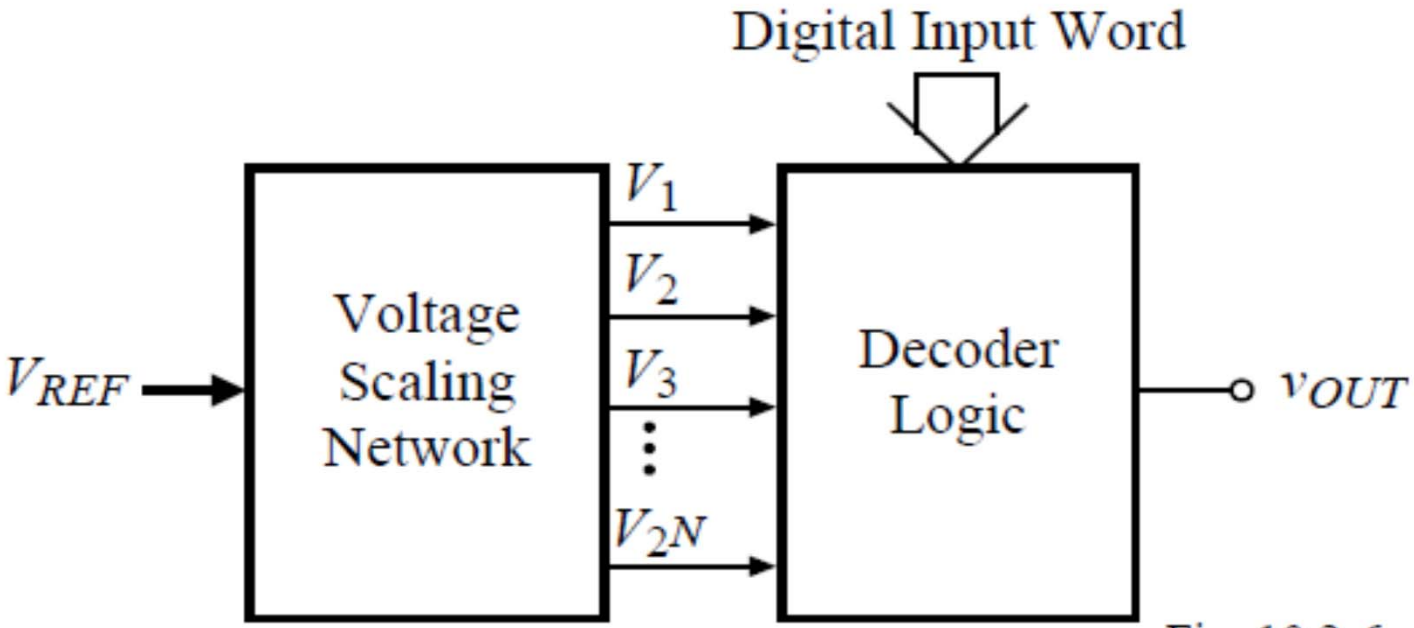
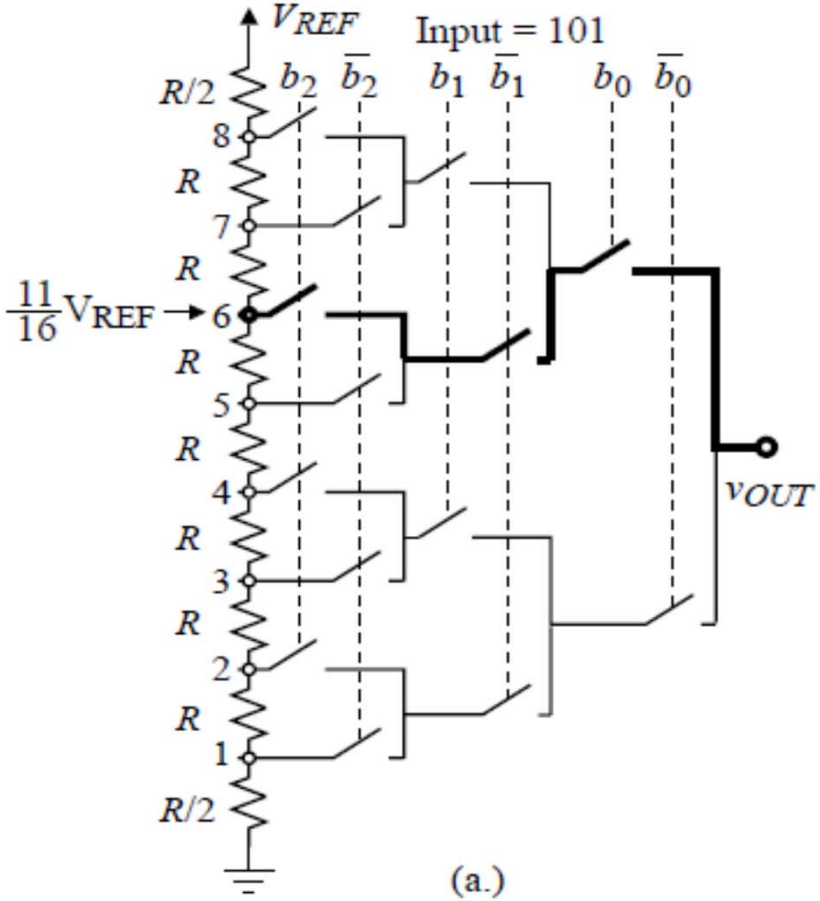
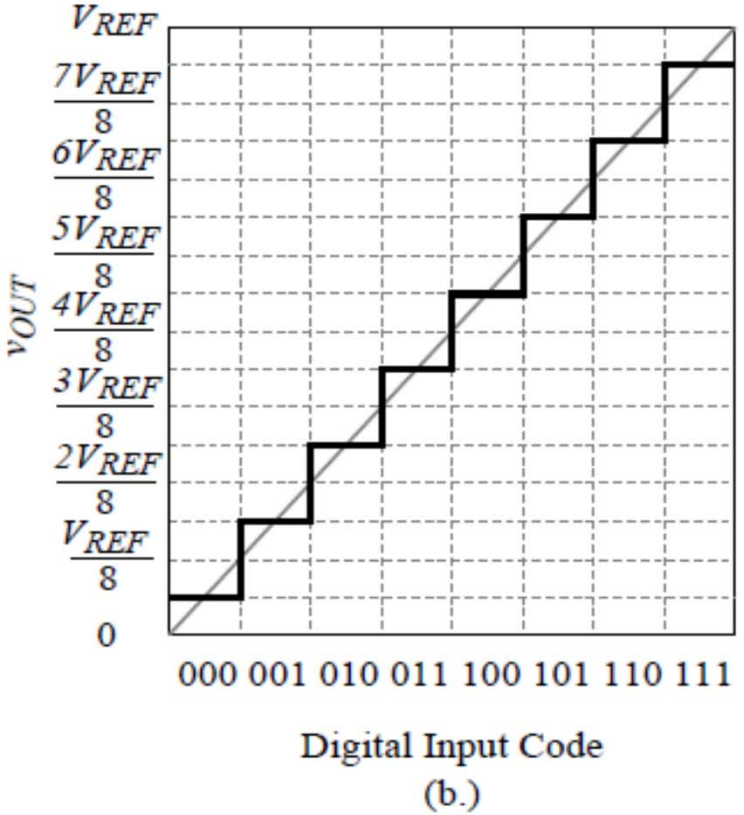


Fig. 10.2-6

Courtesy of Prof. Philip Allen

Example: 3-bit Voltage caling DAC





Courtesy of Prof. Philip Allen

Alternate Realization of the 3-bit DAC

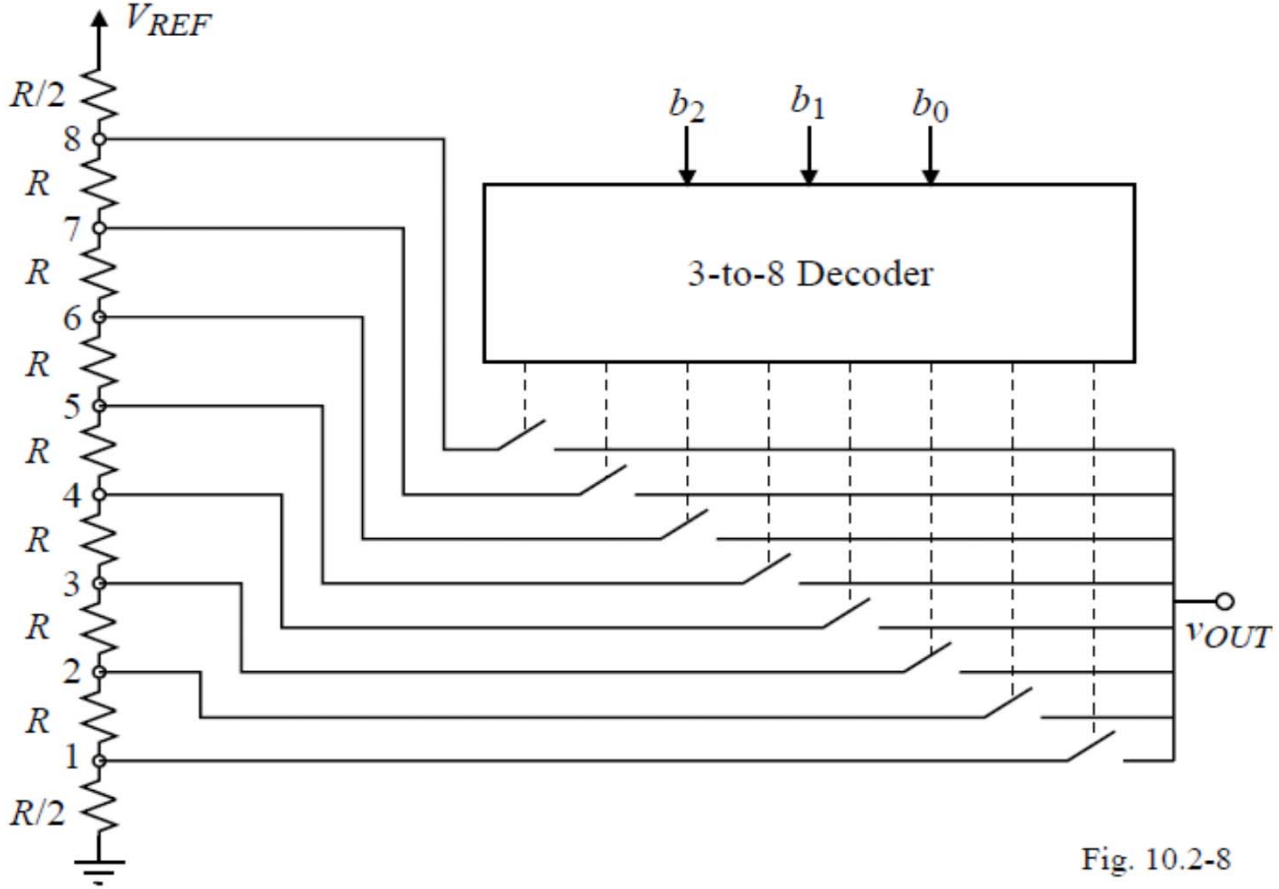


Fig. 10.2-8

Courtesy of Prof. Philip Allen

DAC Input-Output Characteristics

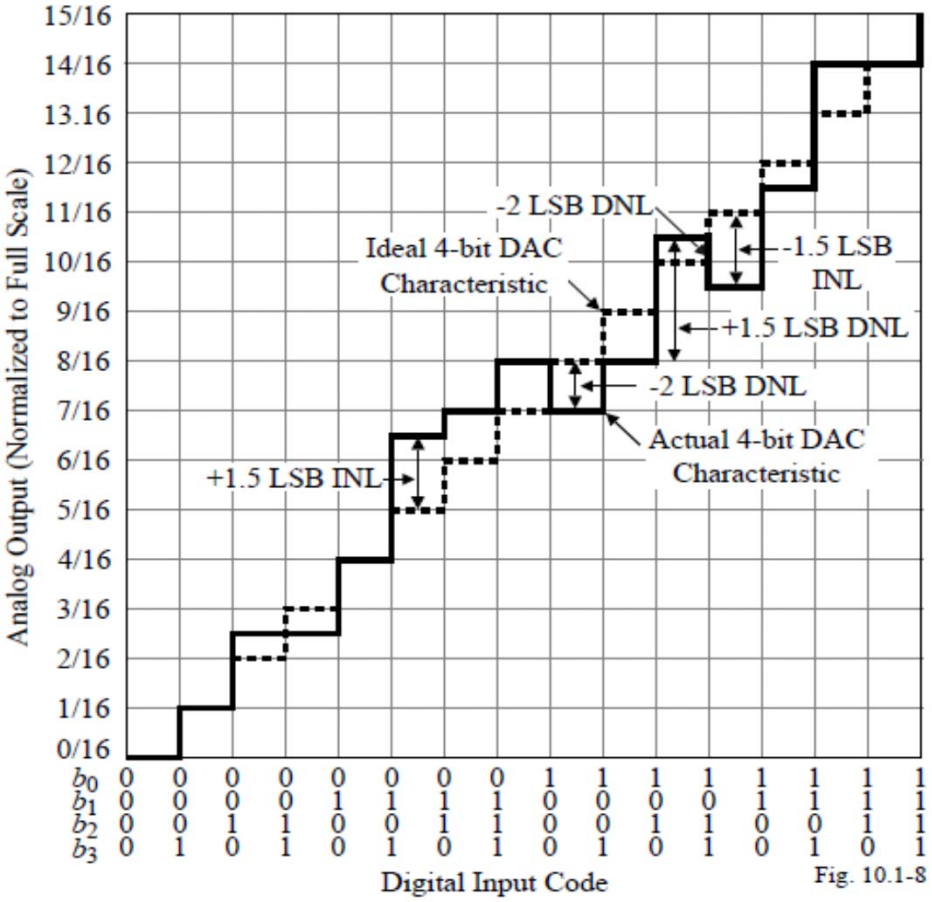


Fig. 10.1-8

Courtesy of Prof. Philip Allen

DAC Timing Requirements

To avoid errors in DACs (and ADCs), $v_{out}(t)$ must be within $\pm 0.5LSB$ of the final value by the end of the conversion time.

Multiple-pole response:

Typically the response is underdamped like the following (see Appendix C of text).

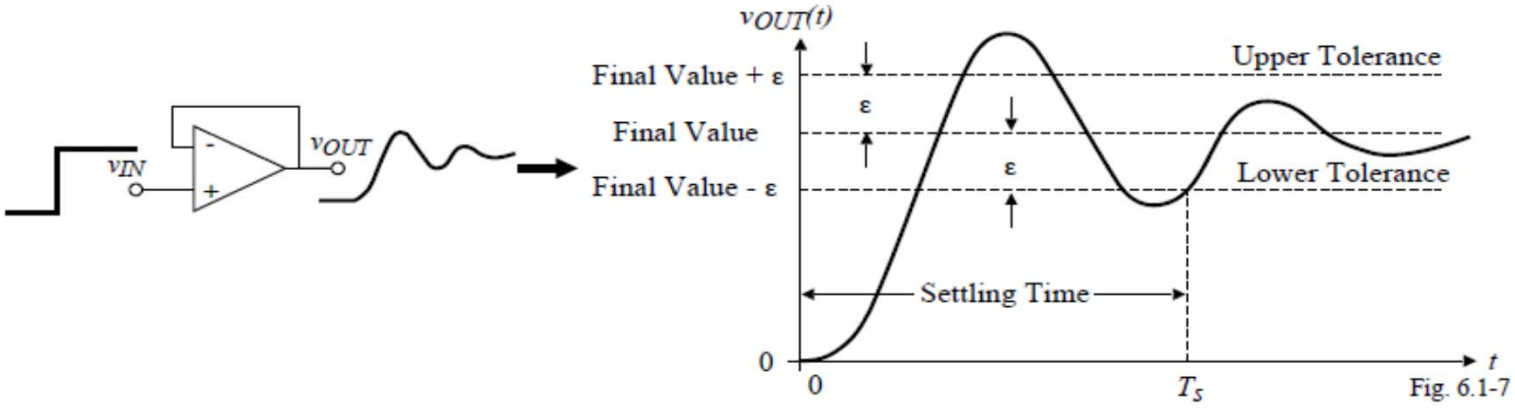
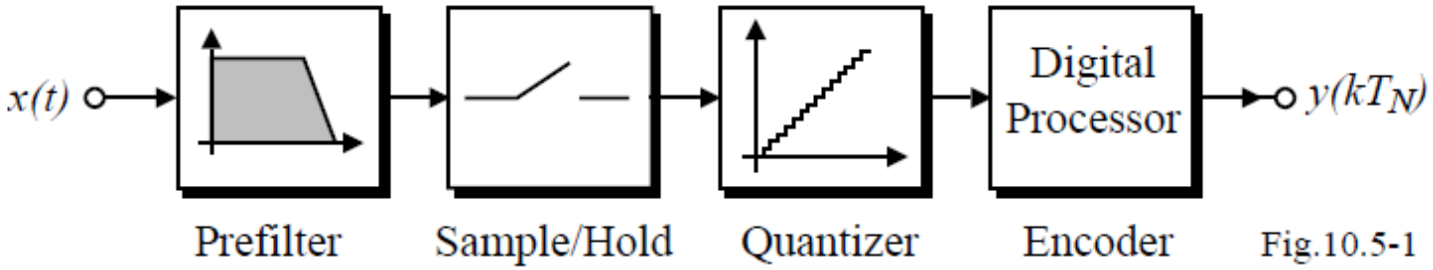


Fig. 6.1-7

Courtesy of Prof. Philip Allen

Basic Analog-to-Digital Converters (ADC)



- Prefilter - Avoids the aliasing of high frequency signals back into the baseband of the ADC
- Sample-and-hold - Maintains the input analog signal constant during conversion
- Quantizer - Finds the subrange that corresponds to the sampled analog input
- Encoder - Encoding of the digital bits corresponding to the subrange

Courtesy of Prof. Philip Allen

Sample and Hold Circuit (Settling Time)

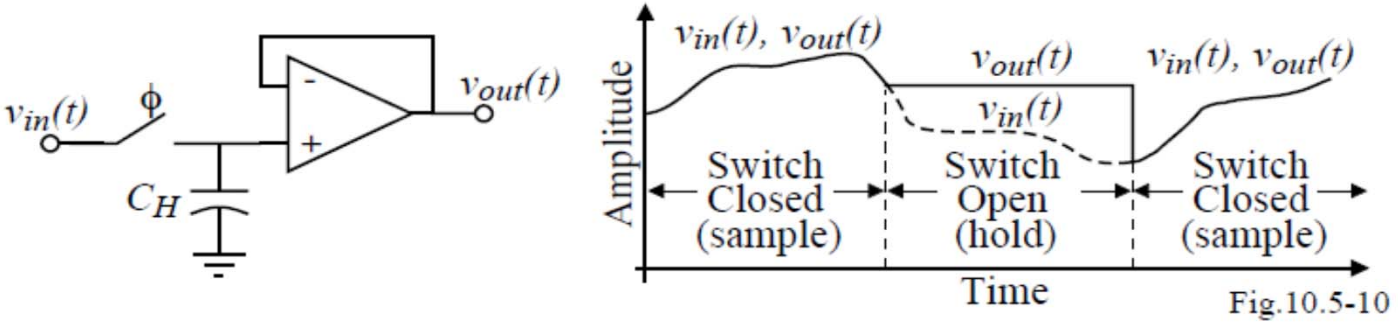


Fig.10.5-10

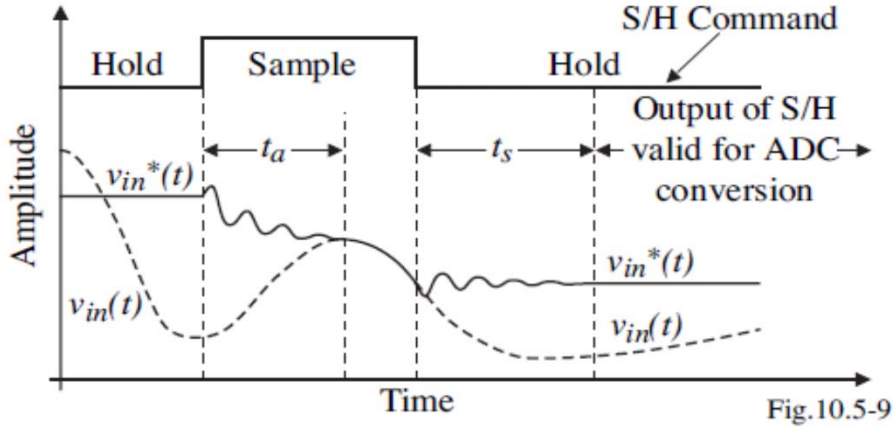


Fig.10.5-9

Courtesy of Prof. Philip Allen

Serial ADC Circuit

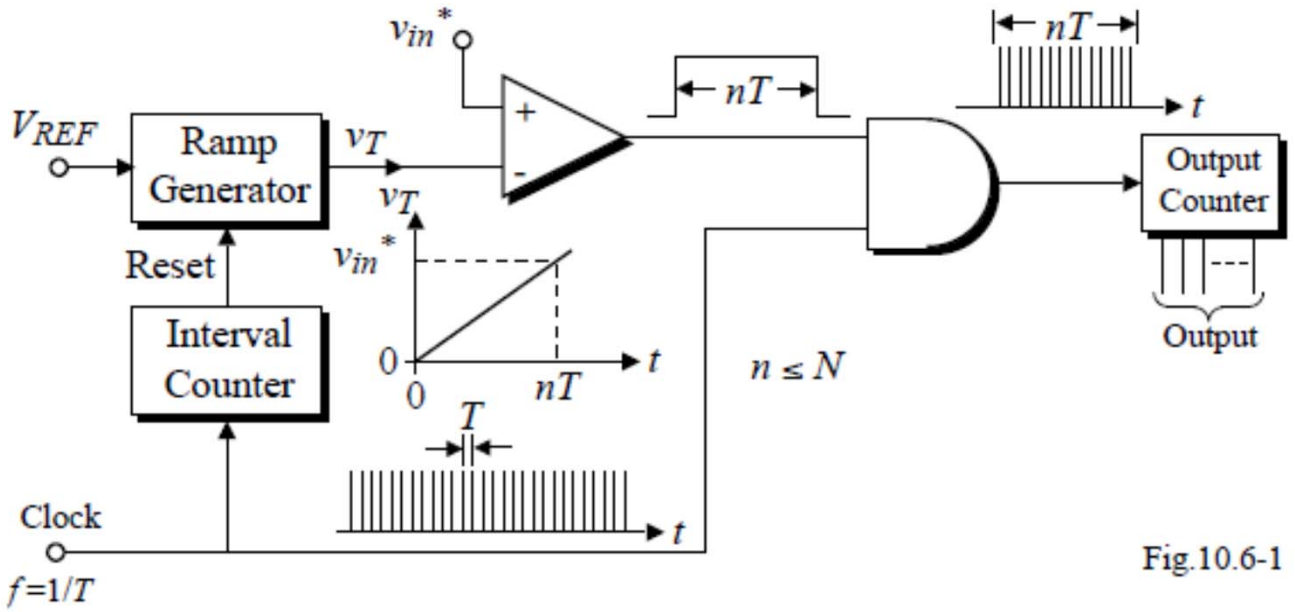


Fig.10.6-1

Attributes:

- Simplicity of operation
- Subject to error in the ramp generator
- Long conversion time $\le 2^N T$

Courtesy of Prof. Philip Allen

Successive Approximation ADC

Successive Approximation Algorithm:

1.) Start with the *MSB* bit and work toward the *LSB* bit.

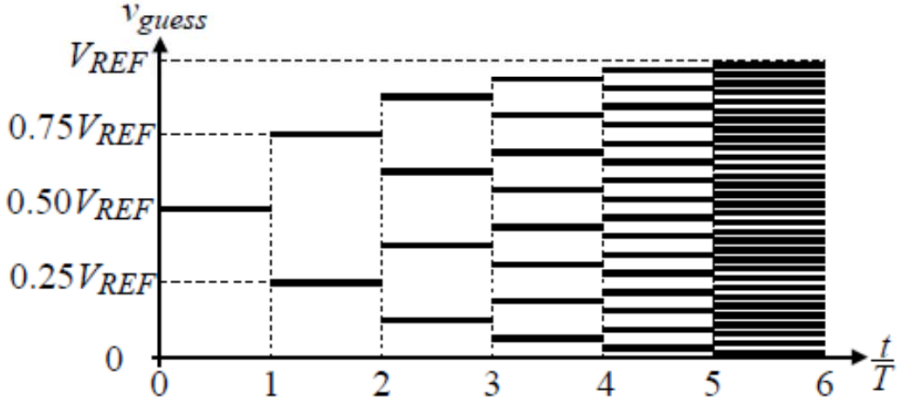
2.) Guess the *MSB* bit as 1.

3.) Apply the digital word 10000.... to a DAC.

4.) Compare the DAC output with the sampled analog input voltage.

5.) If the DAC output is greater, keep the guess of 1. If the DAC output is less, change the guess to 0.

6.) Repeat for the next *MSB*.



Courtesy of Prof. Philip Allen

Implementation of Successive Approximation

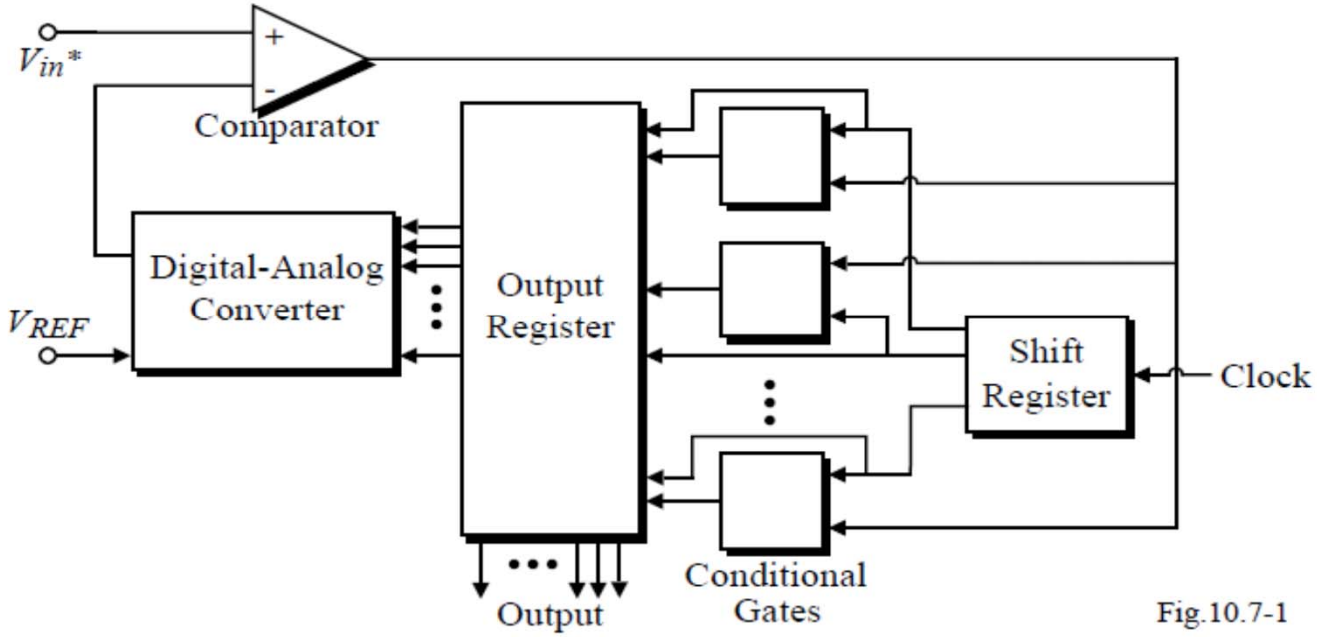


Fig.10.7-1

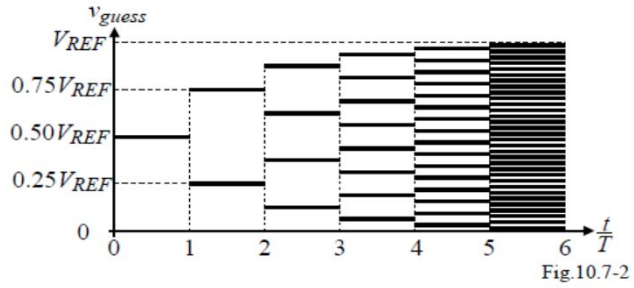


Fig.10.7-2

Courtesy of Prof. Philip Allen

Parallel/Flash ADC Architecture

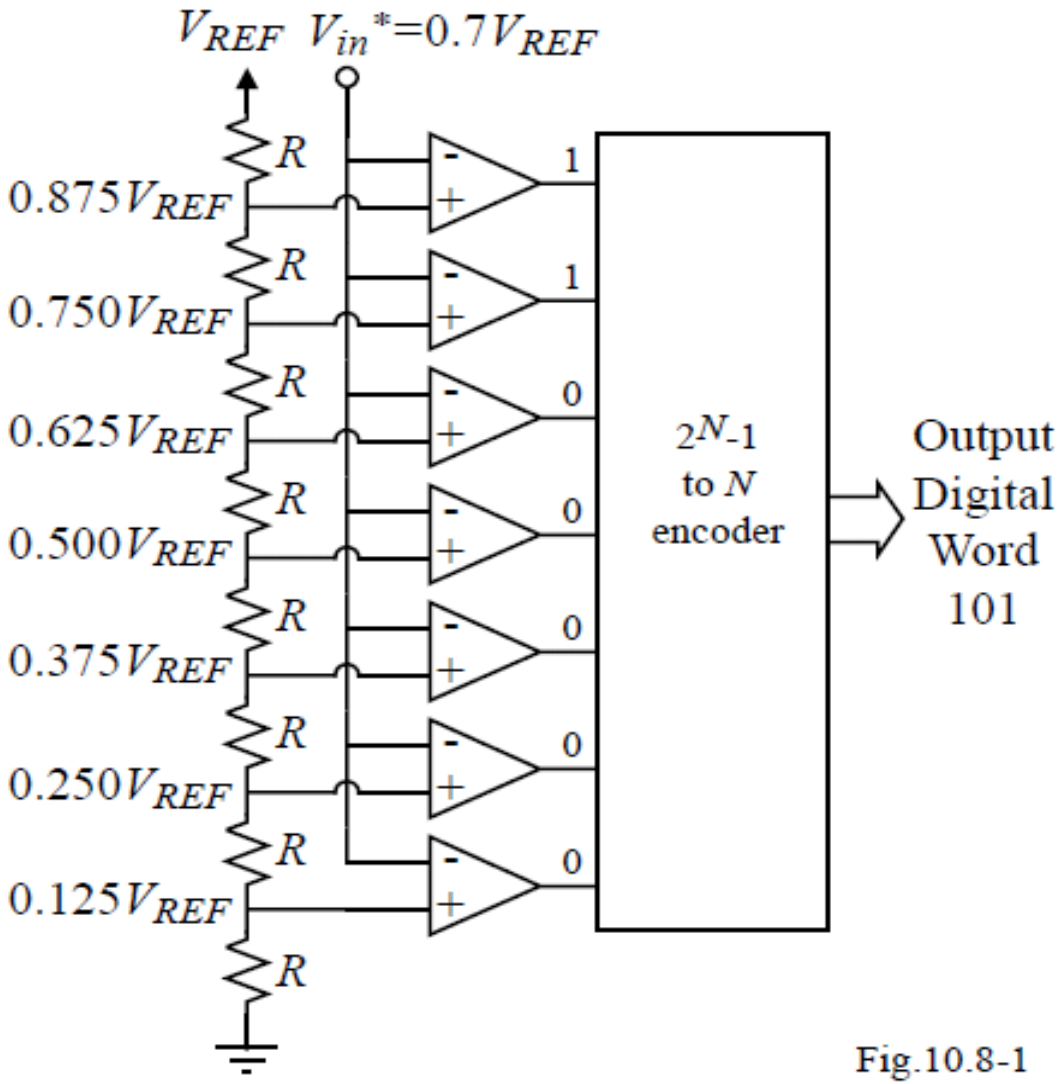


Fig.10.8-1

Courtesy of Prof. Philip Allen