ECE 523/421 – Analog Electronics

Lecture 3: Basic MOSFET Amplifiers II

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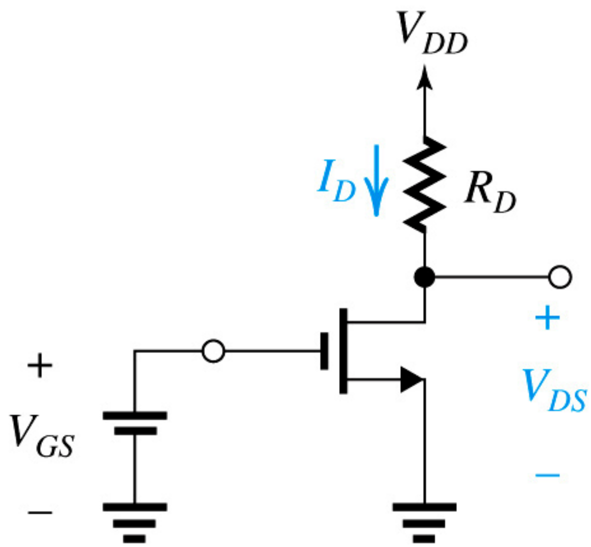
Review of Last Lecture

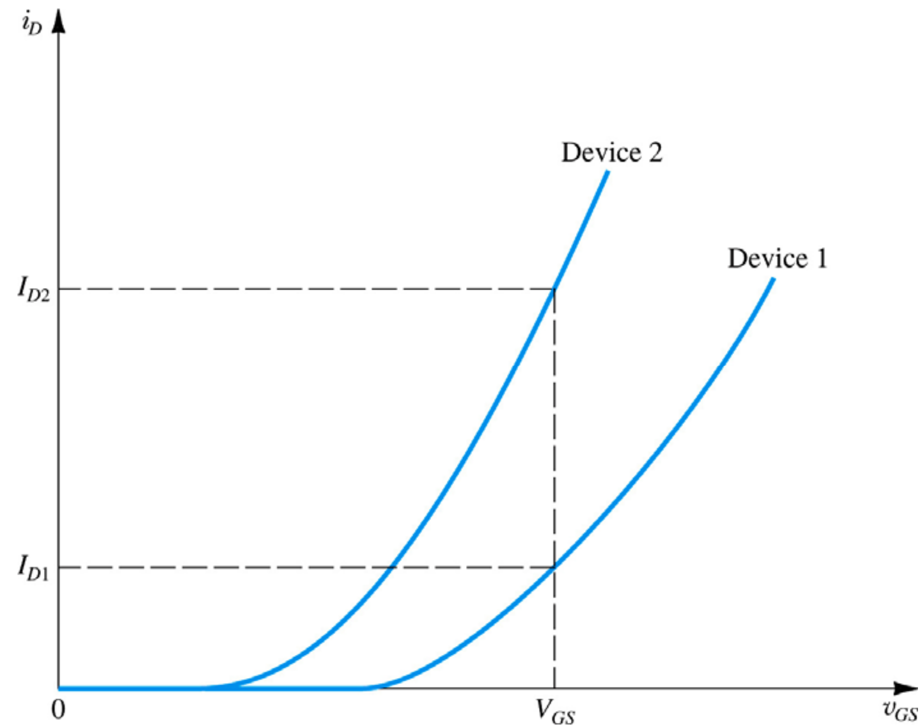
- **MOSFET Biasing for Amplification**
- **MOSFET Small Signal (Π and T Models)**
- **Basic MOSFET Amplifier Configurations (CS, CG, CD)**
- **Examples**

Today's Lecture

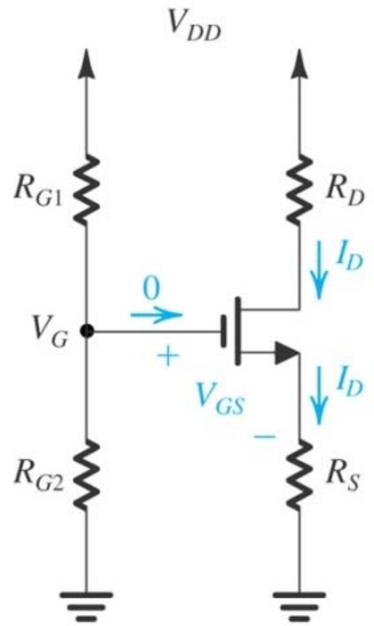
- **Biasing in MOS Amplifier Circuits**
  - **Fix V_{GS} Biasing**
  - **Fix V_{GS} Biasing with Source Resistance**
  - **Drain-to-Gate Feedback Resistor Biasing**
  - **Constant Current Source Biasing**
- **Role of Body Effect in MOS Amplifiers**
- **Temperature Effect**

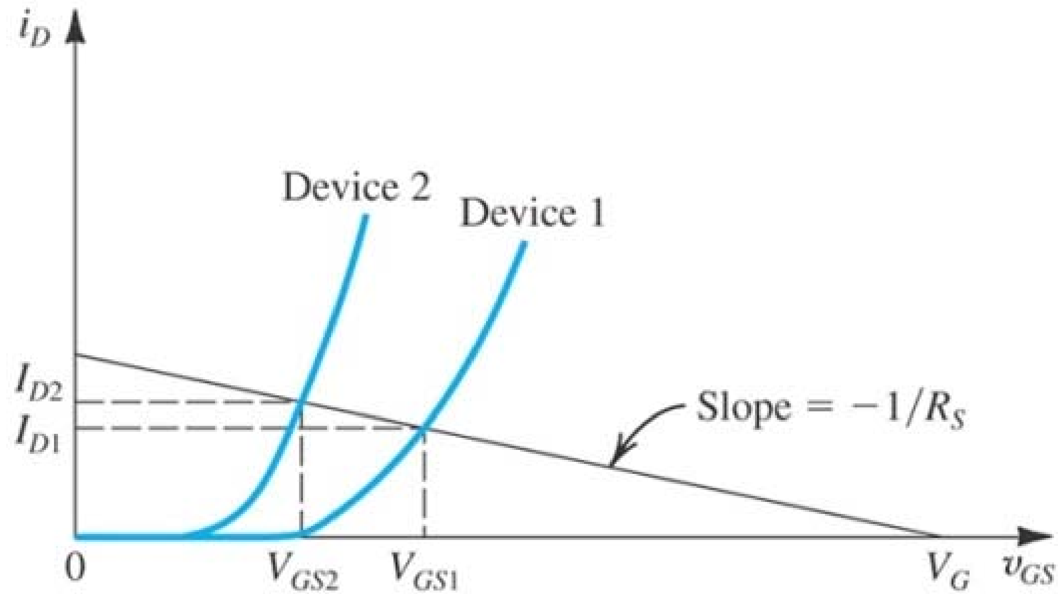
Problem of Fix V_{GS} Biasing





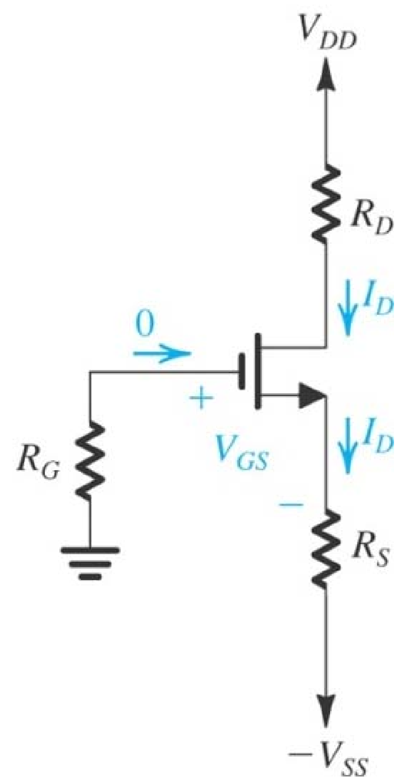
Advantage of R_S in Fix V_{GS} Biasing



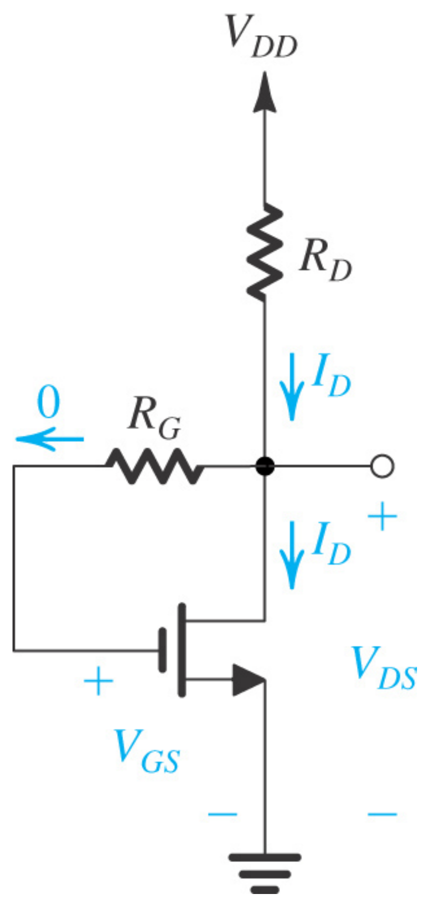


Example: Bias Circuit Design I

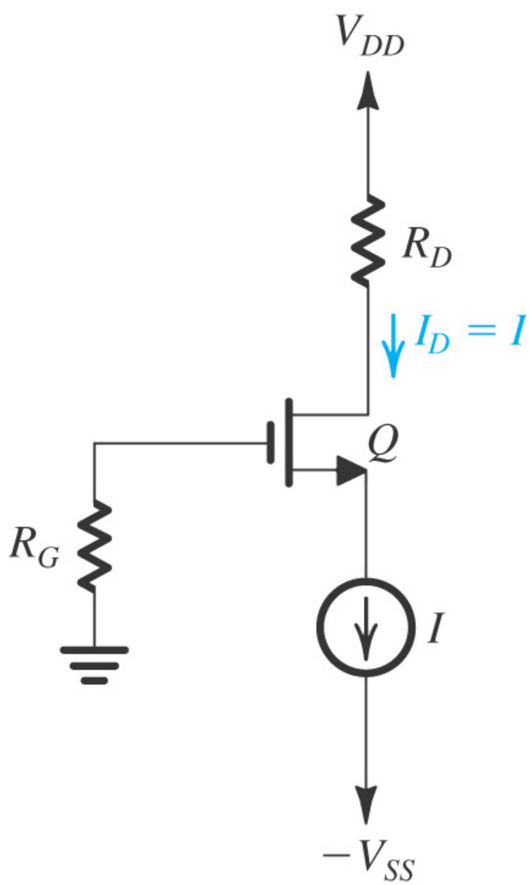
1) Design the following circuit to operate at a dc drain current of 0.5 mA and V_D = +2 V. Let V_t= 1V , $K'_n W/L$ = 1 mA/V^2, and λ=0, V_{DD}=V_{SS}=5 V. Use standard 5% resistor values and give the resulting values of I_D, V_D, and V_S.

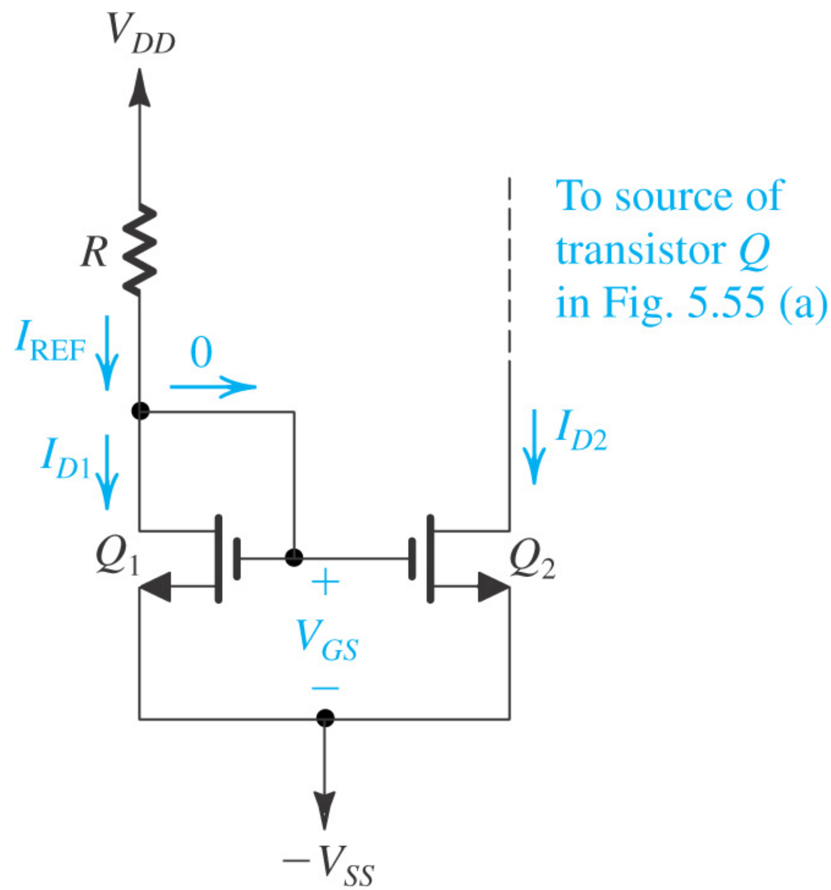


Drain-to-Gate Feedback Biasing



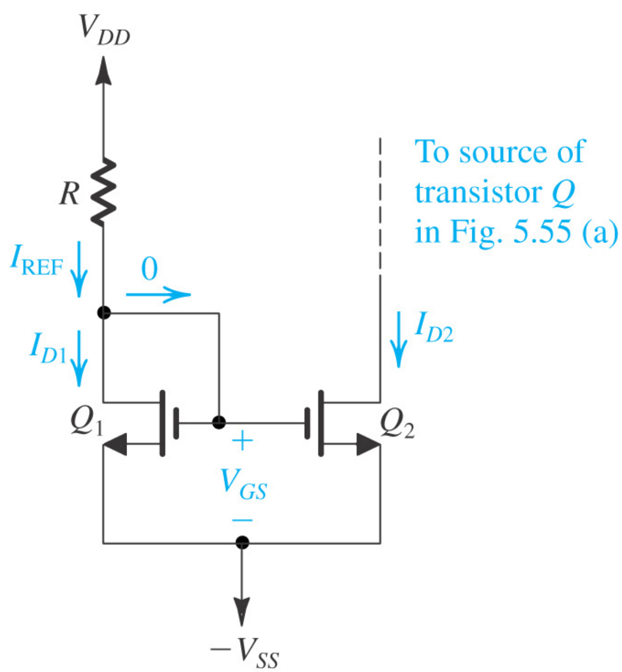
Constant Current Source Biasing



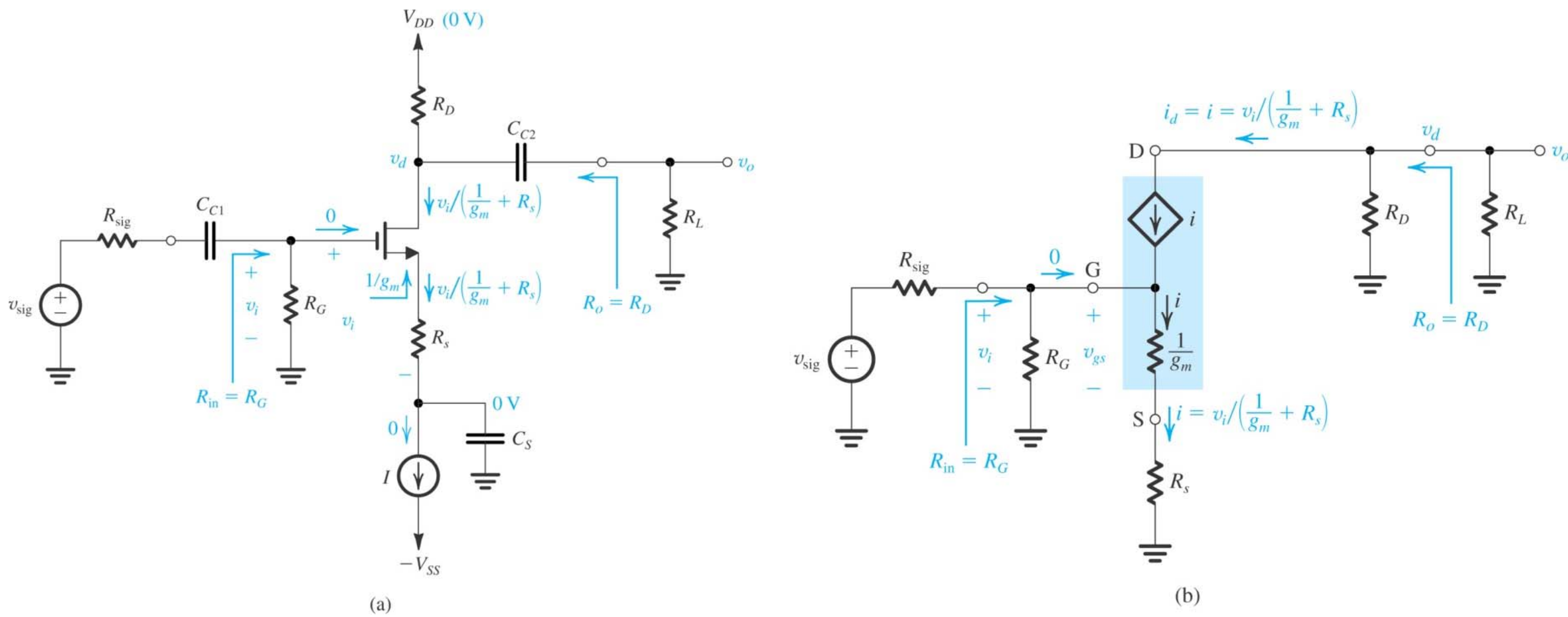


Example: Bias Circuit Design II

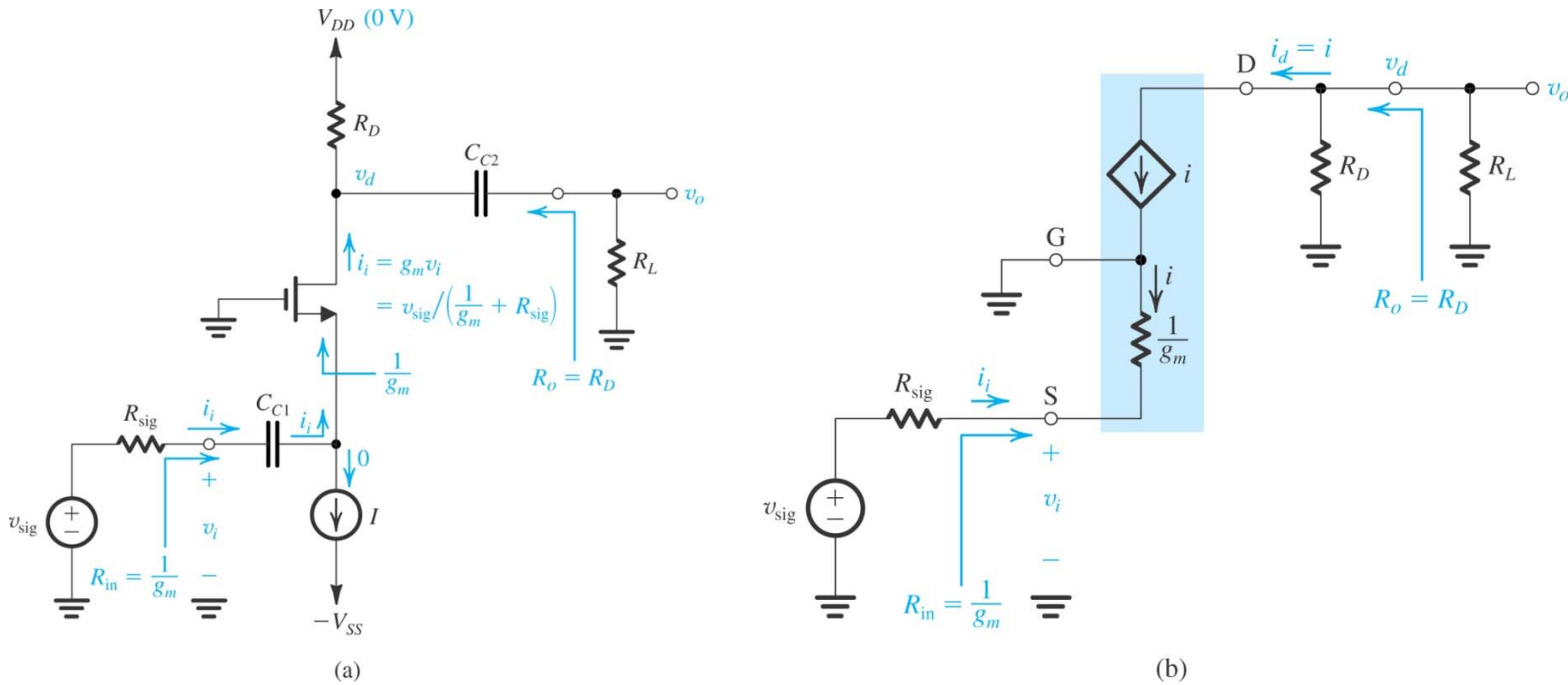
Using two transistors Q_1 and Q_2 having equal lengths but widths related by $W_2/W_1=5$, design the current mirror circuit to obtain I=0.5mA. Let $V_{DD}=-V_{SS}=5V$, $K'_n(W/L)1=0.8mA/V^2$, $V_t=1V$, and $\lambda=0$. Find the required value for R. What is the voltage at eth gate of Q_1 and Q_2? What is the lowest voltage allowed at the drain of Q_2 while Q_2 remains in the saturation region?



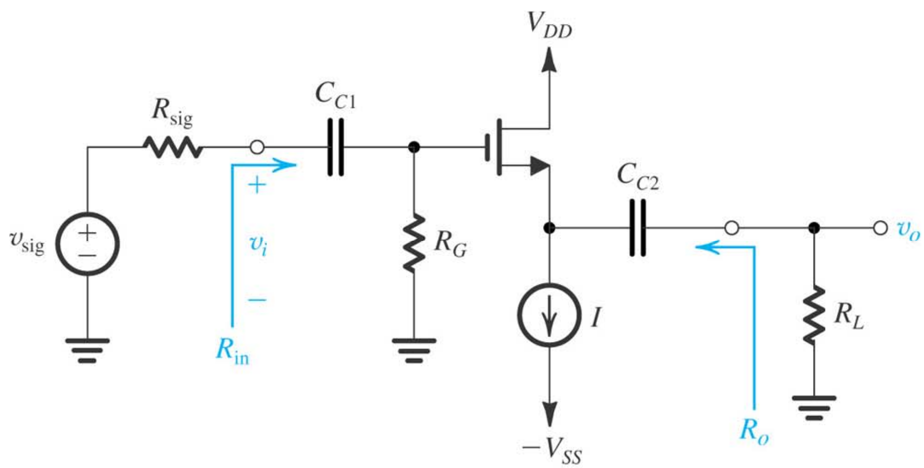
Review of Common-Source Amplifier



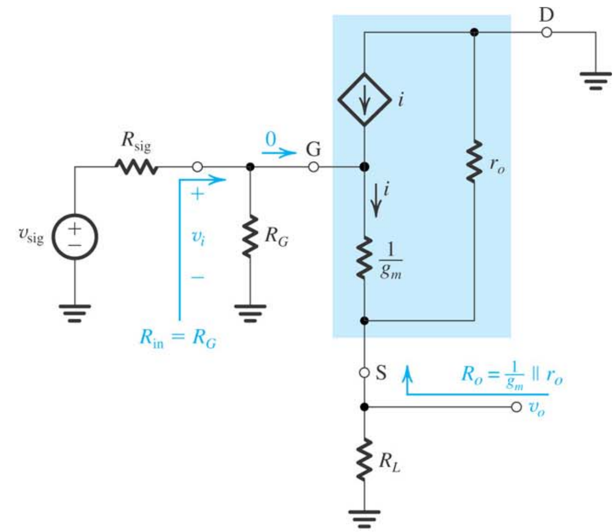
Review of Common-Gate Amplifier



Review of Source Follower Circuit

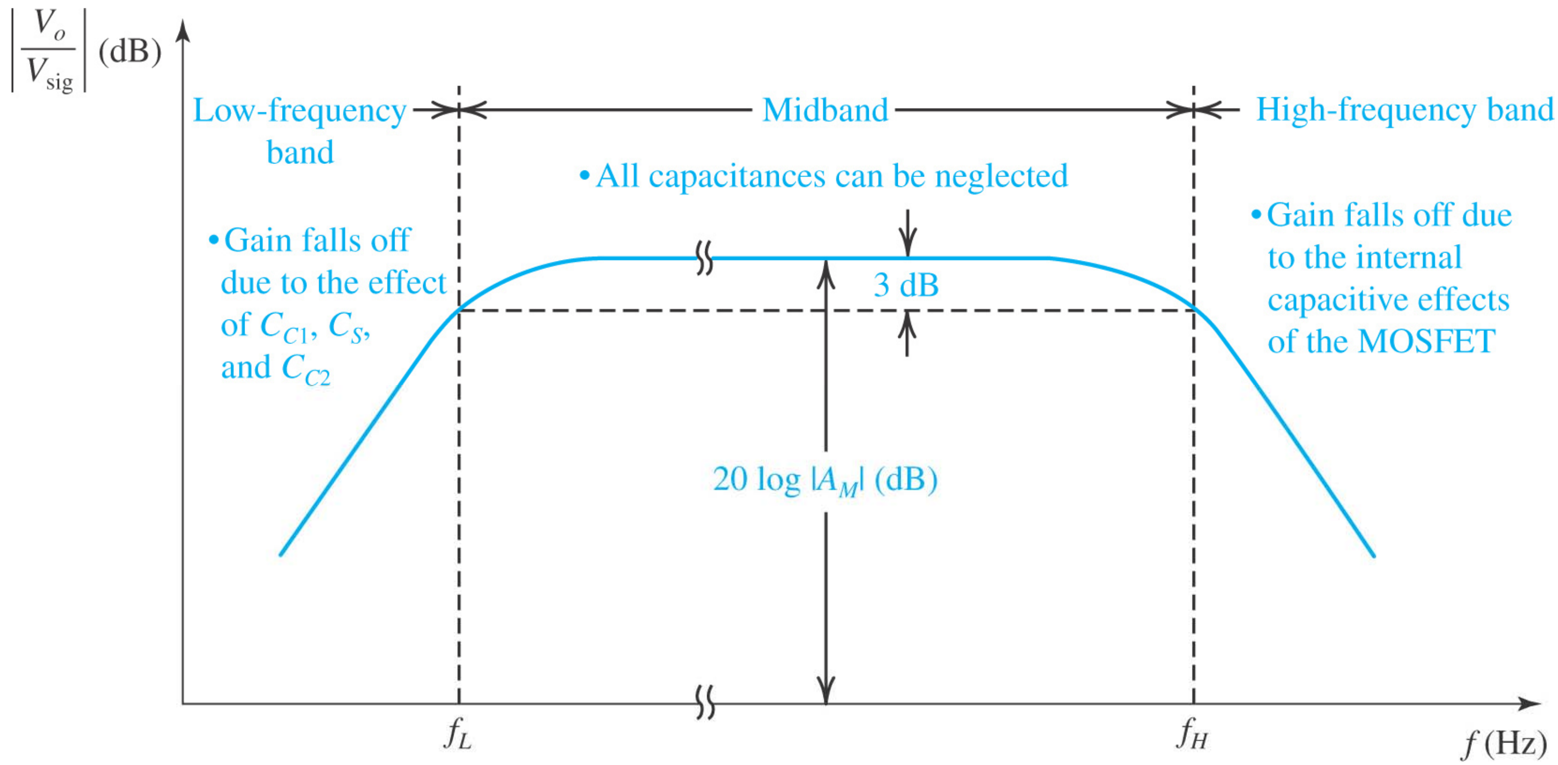


(a)

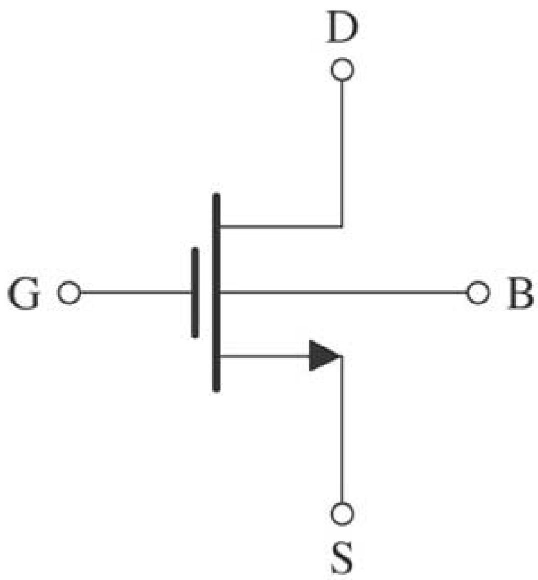


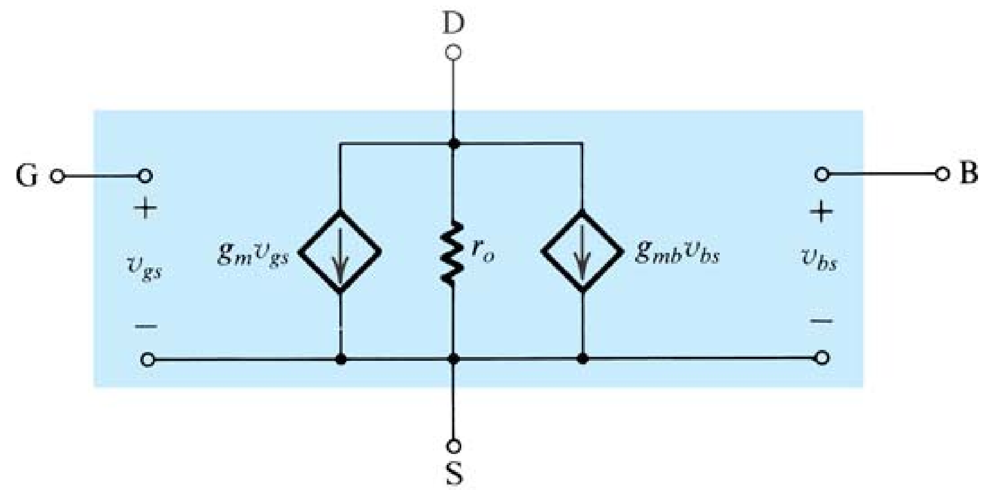
(b)

Quick Review of Frequency Response



Modeling of Body Effect





$$g_{mb} = \chi g_m$$

$$\chi = \frac{\gamma}{2\sqrt{2\varphi_f + V_{SB}}}$$

Temperature Effect

- V_t increases by about 2mV/ºC by temperature increase
- K'_n decreases more by temperature increase
- Overall I_D decreases as temperature increase
- This is an advantage for MOSFET devices (No thermal runaway)