University of New Mexico
Department of Electrical and Computer Engineering

ECE 520 - VLSI Design (spring 2007) Final Exam

Name: Answers Date: May 9, 2007

Note: Only one 8½ inch by 11 inch page equation sheet, ruler, calculator, pencils, and pens are allowed.

1. (10 points) Consider the following CMOS pseudo logic circuits that are used to implement function F.

(a) What is the function F?

(b) Size the NMOS transistors in both circuits such that the fall time delay becomes equivalent to the standard CMOS inverter where $W_P=2W_N$?

(c) What criteria do you use to size PMOS transistor in these circuits?

(d) Indicate which circuit yields to the best performance if the input signal arrival times are ***unknown***?

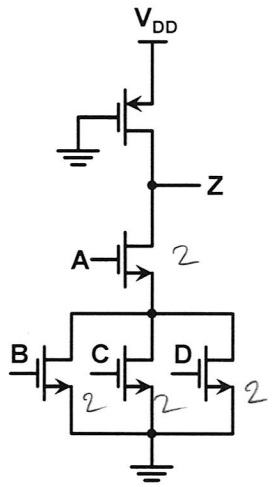
(e) With reference to your answer in part (d), would your choice change if signal A is the first arriving signal? Why or why not?

a) $F=\overline{A(B+C+D)}$

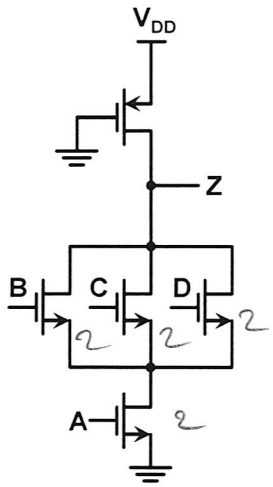
c) V_{OL}

d) Circuit A – lower output cap.

e) Circuit B – lower effective cap.



Circuit A



Circuit B

2. (15 points) The layout of a logic gate is shown below.

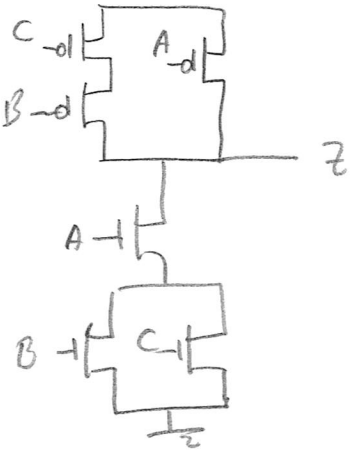
(a) Draw the transistor schematic.

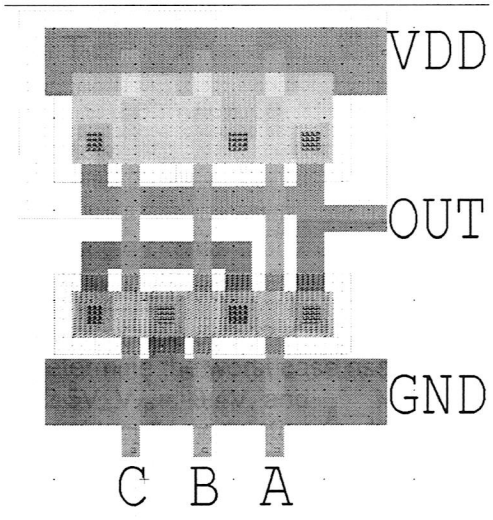
(b) What logic function does this perform?

(c) This layout is not complete. What is missing in this layout?

(d) What input vector (ABC) gives the worst case rise time delay? If the total load capacitance is C_L = 100fF, and $(W/L)_P$ = 5 determine the worst case rise propagation delay, t_{pLH}. Assume that V_{DD} = 2.5V, V_{Tp} = -0.4V, and K'_P = -50μA/V^2. Ignore the body effect, channel length modulation, and intermediate node capacitances. Simplify the problem by assuming that transistors will stay in saturation region during the transition.

(e) What input vector (ABC) gives the worst case leakage current when the output is in logic 1 (high)? If the drain current is 1μA for NMOS at $V_{GS} = V_{Tn}$ and $(W/L)_n$ = 2.5 determine the worst case leakage current when output is high. Assume that V_{DD} = 2.5V, V_{Tn} = 0.4V, and S = 80mV/decade. Ignore the DIBL effect.





a)

b) $Z = \overline{A(B+C)}$

c) Substrate Contact.

d) ABC = 100 , t_{PLH} = 453.5 ps

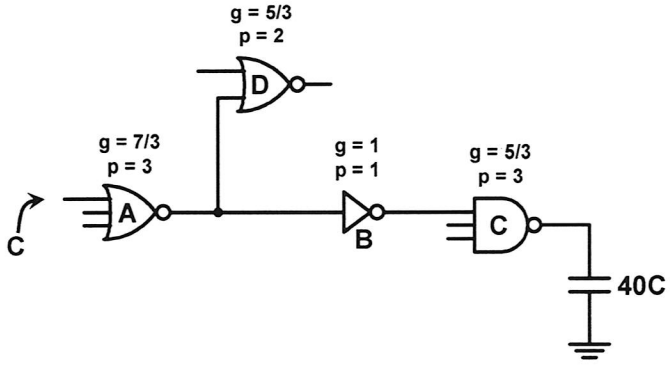
e) ABC < 100 , $I_{leakage}$ = 20 pA

3. (15 points) Use the logical effort technique in the circuit below.

(a) Find the minimum delay.

(b) Optimize gate size for minimum delay.

(c) Determine optimum transistor sizes for minimum delay.



a) $D = 29.37$

b) $C_{in,c} = 8.94$

$C_{in,b} = 4.2$

$C_{in,a} = 1$

4. (20 points) Consider the following sequential circuit with 3 edge-triggered flip-flops and logic blocks A, B, and C. Assume that t_{SU} = 3ns, t_{hold}= 4ns, and t_{C2Q} = 2ns.

(a) Identify all possible paths from Q to D of any flip-flop in this circuit. For logic block A, assume that the delay is the same for both inputs.

(b) If $T_{Logic,A}$ = 3ns, $T_{Logic,B}$ = 4ns, and $T_{Logic,C}$ = 3ns, identify the longest path delay.

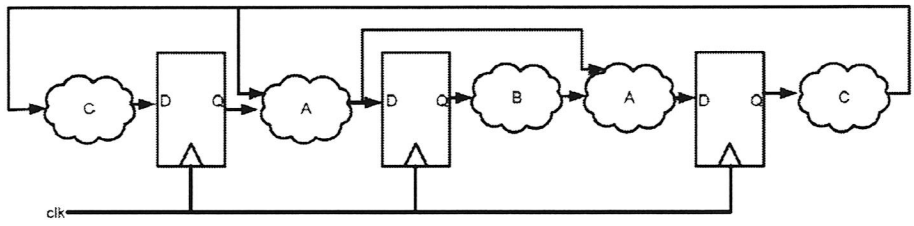
(c) What is the maximum clock frequency at which the circuit can operate correctly?

(d) Does this circuit satisfy the hold time constraint? Why?

(e) To improve the performance, the circuit has been optimized and the logic block delays have been reduced to $T_{Logic,A}$ = 1ns, $T_{Logic,B}$ = 4ns, and $T_{Logic,C}$ = 2ns. Now identify the longest path delay.

(f) What is the maximum clock frequency at which the circuit can operate correctly in this case?

(g) Does the optimized circuit satisfy the hold time constraint? Why?



a) 2C A
C+A B+A
C+2A 2A

b) $C+2A = 9^{ns} \Rightarrow f_{max} = 71.4^{MHz}$

d) $2^{ns} + 3^{ns} > 4^{ns}$ yes

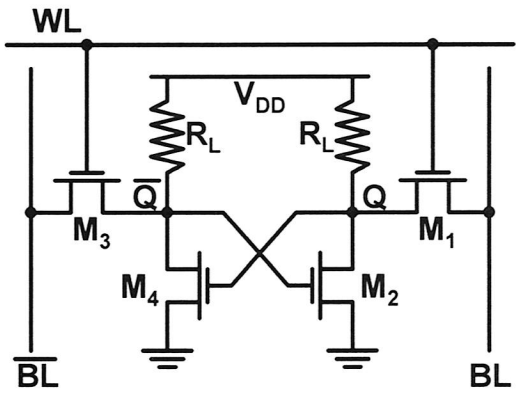
e) $B+A = 5^{ns}$ ~ $f_{max} = 100^{MHz}$

g) no $2^{ns} + 1^{ns} \not> 4^{ns}$

5. (20 points) Consider a resistive load SRAM cell schematic shown below, also known as 4 transistor SRAM cell.

(a) Assume that node Q is in state 1. In order to write a 0 to node Q, bit line, BL, is lowered to 0 V. Determine the minimal size of transistor M_1 so that the cell just flips when this cell is selected. Assume that the switching threshold V_M of the resistive load inverter equals 0.6V. Also, assume that $V_{DD} = 2.5V$, $R_L = 100K\Omega$ $V_{Tn} = 0.4V$, and $K'_n = 100\mu A/V^2$. Ignore body effect.

(b) Now assume that node Q is in state 0. In order to read the cell, both bit lines, BL and $\overline{BL}$, are pre-charged to VDD. Determine the minimum size of transistor M_2 so that the cell does not flip during a read operation. Assume that $(W/L)_1 = 1.2$, which satisfies the constraint in part (a).



a) $\left(\frac{W}{L}\right)_1 = 1.2$

b) $\left(\frac{W}{L}\right)_2 = 1.426$

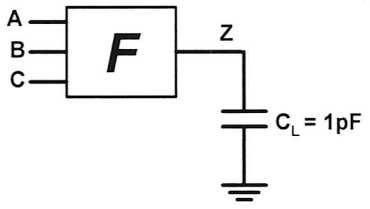
6. (5 points) Logic block F is characterized by the truth table shown below.

(a) Assume that the switching activity at the inputs A, B, and C is 50%. What is the switching activity ($P_{0\to1} + P_{1\to0}$) of the output Z.

(b) If the logic block A derive a load capacitance of C_L=1PF, how much is the dynamic power consumption? Assume that V_{DD} = 2.5V and switching frequency f = 1GHz.

a) $\alpha = 37.5\%$

b) $P = 1.17$ mW



A	B	C	Z
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	0

7. (5 points) Name three sources of clock skew and two sources of clock jitter. What techniques are used to reduce those sources of skew and jitter?

- wire length ⟶ H-tree
- temperature ⟶ uniform Placement
- wire thickness variation ⟶ Dummy fill

- Vdd ⟶ decoupling Cap
- data dependent flip-flop ⟶ differential FF

8. (5 points) Compare NOR and NAND type memories. Explain the advantage and disadvantage of each type.

NOR → faster → Larger → higher capacity

NAND → slower → smaller → lower capacity

9. (5 points) Power consumption of VLSI chips has become a major issue in designing of VLSI chips. Explain three techniques that are used by industry to reduce the power consumption without loosing too much of performance.

- Multicore
- High K
- standby mode
- Multi V_T & V_{DD} Domains