final_exam_08

Friday, May 7, 2021 8:45 PM

University of New Mexico
Department of Electrical and Computer Engineering

ECE 520 - VLSI Design (spring 2008) **Final Exam**

Name: Answers Date: May 14, 2008

Note: Only one 8½ inch by 11 inch page equation sheet, calculator, pencils, and pens are allowed.

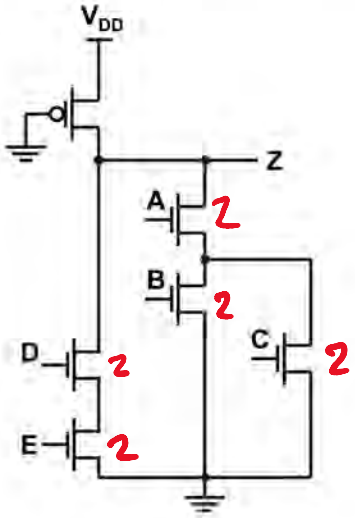
1. (15 points) Consider the following logic gate:
   (a) What kind of logic is this circuit?
   (b) What function does this logic perform?
   (c) Size each NMOS transistor such that the fall time becomes equal to the fall time delay in a unit size inverter?
   (d) What criterion is used to size the PMOS?
   (e) Show the modifications required to make a dynamic CMOS gate out of this circuit.
   (f) Briefly explain how dynamic logic addresses the two disadvantage of the shown circuit.

a) Pseudo Logic

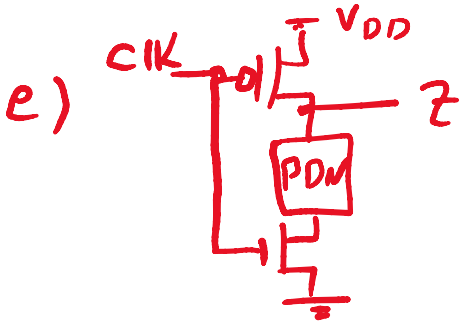
b) $Z = \overline{DE + A(B+C)}$

c) on the diagram

d) PMOS size to get V_{OL}.



e)



f) $V_{OL} = 0$
Eliminate Static Power

2. (15 points) The layout of a logic gate is shown below.

(a) Draw the transistor schematic.

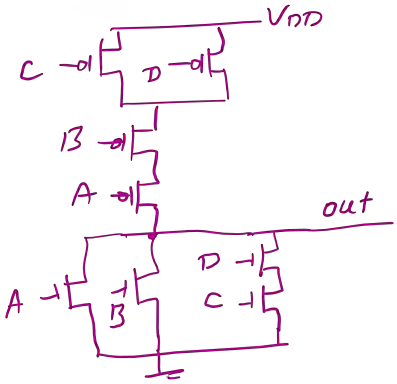
(b) What logic function does this perform?

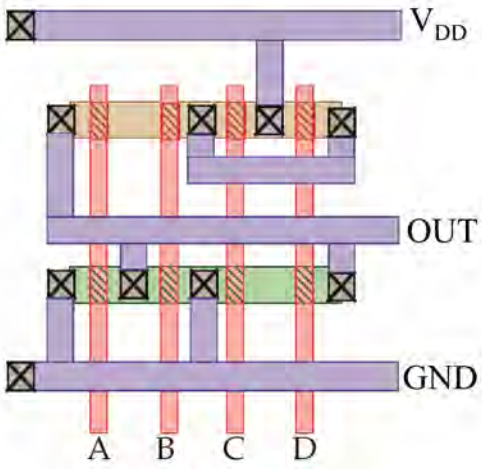
(c) Which input vector gives the worst case leakage? Assume $I_{off(NMOS)}$=25 nA and $I_{off(PMOS)}$=40 nA.

(d) Which input vector gives the largest output high resistance?

(e) Which input vector gives the largest output low resistance?

a)





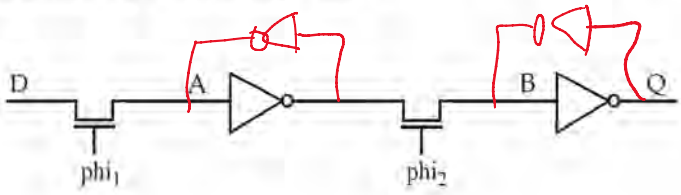
b) $Z = \overline{A+B+CD}$

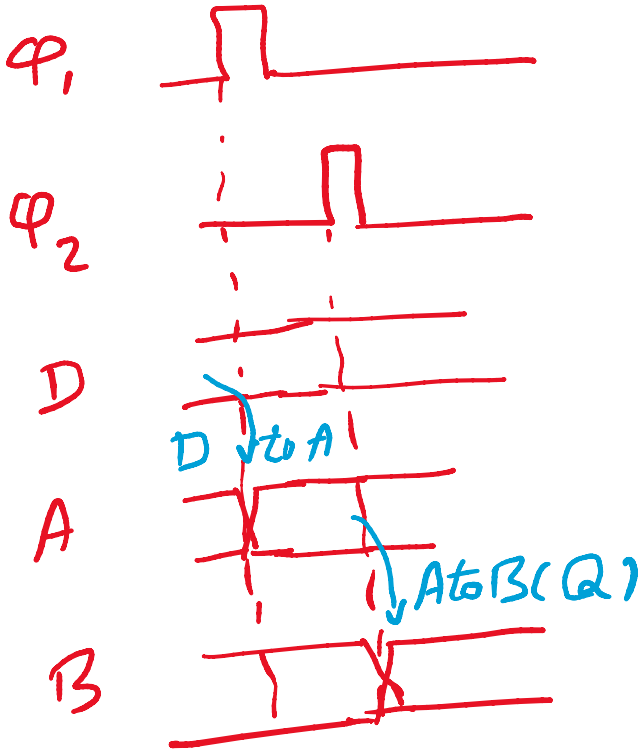
c) ABCD = 0011

d) ABCD = 0010 or 0001

e) ABCD = 0011

3. (10 points) In the following circuit, assume that phi1 and phi2 are non-overlapping clocks. Briefly explain how this circuit can be used to implement a D flip-flop using a timing diagram with D, phi1, phi2, and Q. Modify this gate so that the degraded logic value at nodes A and B is fully restored.





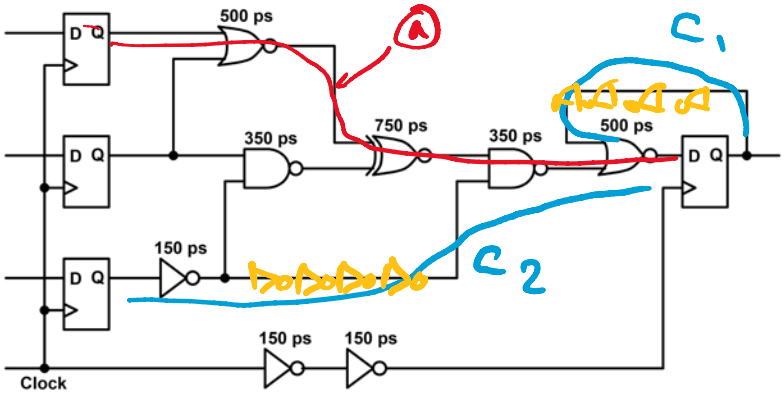
4. (15 points) Consider the following sequential circuit with 4 edge-triggered flip-flops and some logic gates. Assume that t_{SU} = 3 ns, t_{hold}= 2 ns, and t_{C2Q} = 1 ns.

(a) Identify the critical path on the schematic.

(b) What is the maximum operating frequency of this circuit?

(c) Identify the path with hold time violation on the schematic.

(d) How do you modify the circuit to avoid the hold time violation without any penalty on the operating frequency? add inverters



a) critical Path : $t_{logic} = 500 + 750 + 350 + 500$
$= 2.1^{ns}$

b) $T > t_{C2Q} + t_{logic} + t_{SU} - t_{SKEW}$

$T > 1^{ns} + 2.1^{ns} + 3^{ns} - 0.3^{ns} = 5.8^{ns}$

$\Rightarrow f_{max} = 172\ MHz$

c) C_1: $t_{hold} < t_{C2Q} + t_{logic} - t_{SKEW}$ hold time

$2^{ns} \not< 1^{ns} + 0.5^{ns} - 0$ → violation

C_2: $t_{hold} < t_{C2Q} + t_{logic} - t_{SKEW}$ hold time

$2^{ns} \not< 1^{ns} + 1^{ns} - 0.3^{ns}$ → violation

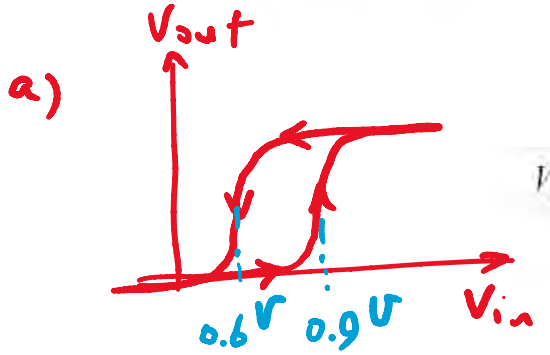
5. (15 points) Consider the circuit below. The inverter is ideal, with $V_M=V_{DD}/2$ and infinite slope. The transistors have V_{Tn} = 0.4 V, k'_n = 120 μA/V^2, V_{Tp} = -0.4 V, and k'_p = 40 μA/V^2. M1 has $(W/L)_1$=1. Ignore all other parasitic effects in the transistors.

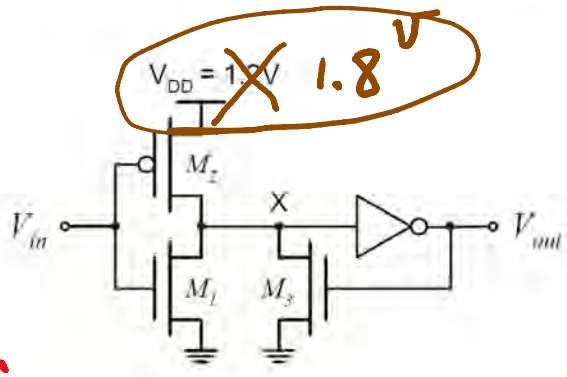
(a) As V_{in} goes from 0 to V_{DD} and back to 0 explain the sequence of events which makes this circuit operate as a Schmitt Trigger. Plot V_{out} versus V_{in}.

(b) Find the value of $(W/L)_2$ such that when V_{IN} increases from 0 to V_{DD} the output will switch at V_{in} = 0.9V.

(c) Find the value of $(W/L)_3$ such that when V_{IN} decreases from V_{DD} to 0 the output will switch at V_{in} = 0.6V.

a)





b) M3: OFF $\quad \frac{K'_n}{2}\left(\frac{W}{L}\right)_1(V_M-V_{Tn})^2 = \frac{K'_p}{2}\left(\frac{W}{L}\right)_2(V_{DD}-V_M-|V_{Tp}|)^2$

$\frac{120}{2}\times 1\times(0.9-0.4)^2 = \frac{40}{2}\left(\frac{W}{L}\right)_2(1.8-0.9-0.4)^2$

$\Rightarrow \left(\frac{W}{L}\right)_2 = 3$

c) M3: ON $\quad \frac{K'_n}{2}\left[\left(\frac{W}{L}\right)_1+\left(\frac{W}{L}\right)_3\right](V_M-V_{Tn})^2 = \frac{K'_p}{2}\left(\frac{W}{L}\right)_2(V_{DD}-V_M-|V_{Tp}|)^2$

$\frac{120}{2}\times\left[1+\left(\frac{W}{L}\right)_3\right]\times(0.6-0.4)^2 = \frac{40}{2}\times 3\times(1.8-0.6-0.4)^2$

$\Rightarrow \left(\frac{W}{L}\right)_3 = 15$

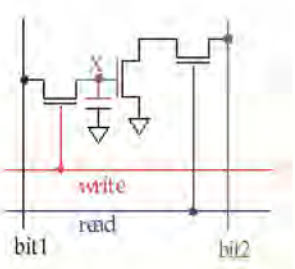
6. (15 points) The following circuit is a modified DRAM cell with three transistors (3T DRAM).

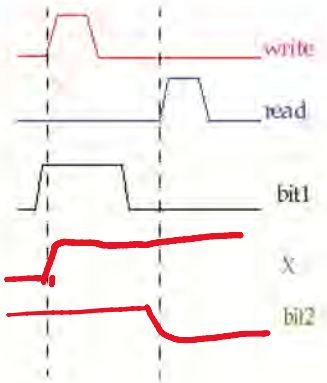
(a) Show the electrical behavior of node X and bit 2 using the timing diagram for write, read, and bit 1 shown below. Assume that the cell originally stores 0 and bit 2 is precharged to V_{DD}-V_T.

(b) Does this cell require refreshing? Why?

(c) Is the operation of reading this cell destructive? Why?

(d) Briefly explain the advantage and disadvantage of this 3T DRAM cell versus 1T DRAM cell.





b) No. The read operation does not disturb the charge in C.

c)

3T-DRAM	1T-DRAM
Larger	smaller
Non-destructive Read	Destructive Read
Needs seperate Read and write Line	Needs only one Word Line
more Complex layout	simpler layout

7. (5 points) Briefly explain how mesh clock distribution provides clock a VLSI chip.

(a) What are the advantages of mesh clock distribution network versus balanced tree?

(b) What are the disadvantages of mesh clock distribution network versus balanced tree?

a) mesh distribution has less skew

b) larger Cap ⇝ more Power dissipation
needs a lot of wiring resource

8. (5 points) With respect to Non-volatile Read-Write memories, there are three types, EPROM, EEPROM, and Flash.

(a) What advantage does EEPROM have over UV erasable EPROM?

(b) What advantage does UV eraseable EPROM have over EEPROM?

(c) Why is Flash EEPROM better than UV eraseable EPROM and EEPROM?

a) No need for uv light to erase

b) No over-erase issue → easier
to implement

c) flash is faster and denser
due to advance design techniques
such as multiple V_T.

9. (5 points) Technology scaling has improved the performance, density, and power of VLSI chips. However, some reliability issues, such as hot electrons, become more serious with technology scaling.

(a) Briefly explain how hot electrons can impact the performance of VLSI chips over time.

(b) What do you recommend to reduce the hot electrons in scaled CMOS technology?

a) Hot electrons stack in the gate oxide ⇝ increases V_T ⇝ reduces Performance

b) increase L (reduces short channel effects)

or reduce V_{DD} (reduces Pulling up electric field)