midterm_08_sol

Thursday, March 18, 2021 1:02 PM

University of New Mexico
Department of Electrical and Computer Engineering

ECE 520 - VLSI Design (spring 2008) **Midterm Exam**

Name: Answers Date: March 26, 2008

Note: Only one 8½ inch by 11 inch page equation sheet, ruler, calculator, pencils, and pens are allowed.

1. (10 points) We have contacted a foundry to manufacture our VLSI test chip at 45nm technology. According to their device specs, the threshold voltage of NMOS is 0.30V when channel length L=45nm. However, when we simulate NMOS with L=75nm in this technology, SPICE simulations show that the threshold voltage is 0.35V. Explain why?

This is due to threshold voltage roll-off.

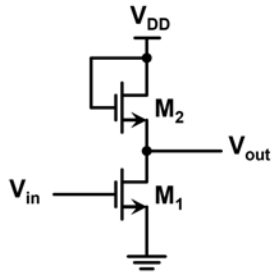
2. (20 points) Prior to CMOS technology, the logic gates were made of NMOS device only. The following circuit shows an inverter using NMOS only.

(a) Assume that $V_T = 1V$, $K'_n = 100\ \mu A/V^2$, $(W/L)_1 = (W/L)_2 = 10$, and $V_{DD} = 5V$. Find V_{OL} and V_{OH} of this inverter. Ignore body effect.

(b) Write the expression for ***input*** and ***output*** parasitic capacitance of this inverter as a function of C_{OX}, C_J, C_{JSW}, A_D, P_D, C_{GSOV}, C_{GDOV} of M_1 and M_2?

a) $V_{OH} = 4\ V$

$V_{OL} = 1.17\ V$



b) $C_{in} = C_{GDOV_1} + C_{GSOV_1} + W_1 C_{ox} L_{eff}$

$C_{out} = 2 C_{GDOV_1} + K_{eq_1}(C_{j1} A_{D_1} + C_{jsw_1} P_{D_1})$

$+ \frac{2}{3} W_2 C_{ox} L_{eff}$

3. (30 points) For a MOSFET operating in the subthreshold regime ($V_{GS} < V_T$), the reduction in gate voltage needed to reduce the drain current by one decade is defined as the "subthreshold swing", S, where

$$S = \frac{kT}{q} Ln(10)\left(1 + \frac{C_{Dep}}{C_{OX}}\right),$$

The unit of S is mV/decade.

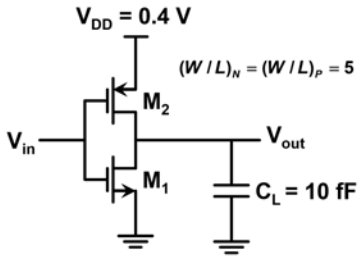
(a) Find S at room temperature for NMOS and PMOS devices. Assume that gate oxide thickness is $t_{OX} = 2\ nm$ for both NMOS and PMOS, and channel depletion depth in NMOS is $W_{Dep} = 30\ nm$ and in PMOS is $W_{Dep} = 15\ nm$ ($\varepsilon_{sio2} = 3.9$ and $\varepsilon_{si} = 11.9$).

(b) These devices are used in an inverter that operates in subthreshold region, where V_{DD} is less than device threshold voltages. Using the drain current equation at subthreshold region, calculate the leakage currents when the inverter input is set to **0** and **1**. The device measurements indicate that for the device sizes used in the inverter circuit, $I_{O(NMOS)} = 15\ \mu A$ and $I_{O(PMOS)} = 10\ \mu A$. Assume that $V_{DD} = 0.4V$, $V_{Tn} = |V_{Tp}| = 0.5V$ and $\lambda_n \approx \lambda_p \approx 0$.

(c) Using the drain current equation at subthreshold region, compute the rise and fall propagation delays (50% delays) of the inverter, t_{PLH} and t_{PHL}. Assume that the total load capacitance of the inverter is $10\ fF$.

Hint: Drain current equation at subthreshold region is:

$$I_{DS} = I_O e^{\frac{V_{GS}-V_T}{nKT/q}}\left(1 - e^{\frac{-V_{DS}}{KT/q}}\right)(1 + \lambda V_{DS})$$



a) NMOS: $S = 72$ mV/dec

PMOS: $S = 84.2$ mV/dec

b) $I_{DS_n} = 1.645$ PA

$I_{DS_P} = 11.57$ PA

This page is left blank to be used for problem 3

c) $t_{PHL} = 3.28$ ns

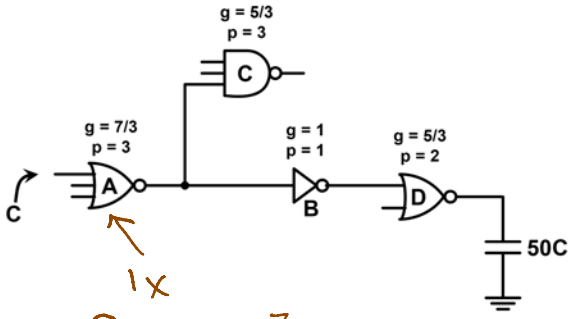
$t_{PLH} = 3.06$ ns

4. (15 points) Use the logical effort technique in the circuit below.

(a) Find the minimum delay.

(b) Optimize gate size for minimum delay.

(c) Determine optimum transistor sizes for minimum delay.



a) $D_{min} = 30.1$ $\quad C = 1 \times g_1 = \frac{7}{3}$

b) $C_{in}(D) = 10.37C$

$C_{in}(B) = 1.29C$

$C_{in}(A) = 1.0C$

c) $S_D = \frac{10.37 \times (7/3)}{5/3} = 14.5\,x$

$S_B = \frac{1.29 \times (7/3)}{1} = 3\,x$

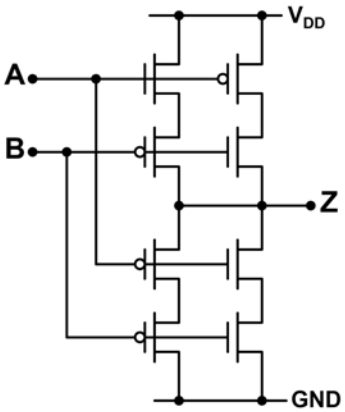
$S_A = \frac{1 \times (7/3)}{7/3} = 1\,x$

5. (15 points) Consider the following logic circuit that is used to implement function Z.

(a) What is the function Z? Explain how the circuit operates.

(b) Although the circuit appears digitally correct, it operates slowly. Moreover, when two of these gates are cascaded, the results are unreliable. Suggest explanations for these two problems.

(c) Propose a modification to the circuit which retains the general design but introduces two pairs of additional inverters to address the problems.



a) $Z = A \oplus B$

b) use of NMOS for Pullup and PMOS for Pulldown.

c) use of $\bar{A}$ and $\bar{B}$ when needed, instead.

6. (5 points) What is "Bent Gate"? What is the advantage and difficulty of using bent gate?

Bent Gate is a layout technique to reduce transistor area.

7. (5 points) What is STI? How does it help to scale CMOS technology?

shallow trench insulator.
It needs less space to isolate MOSFETs.